



Migration Note

EON Flash EN25P80 to EN25Q80A



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1. INTRODUCTION

The application note introduces how to implement a system design from EON EN25P80 Flash to Eon EN25Q80A Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the features of these two devices.

Features	EN25P80	EN25Q80A
voltage range	2.7 ~ 3.6	2.7 ~ 3.6
SPI frequency	75MHz (standard mode)	100MHz (standard mode) 80MHz @ dual & quad mode
Secured Silicon Sector region	N/A	256 Byte
Sector Architecture	Uniform 16 sectors of 64K byte	Uniform 128 sectors of 4K byte / 16 block of 64K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
Minimum endurance cycle	100K	100K
Package	8-pin 200mil SOP 8 contact VDFN	8-pin 150mil / 200mil SOP 8 contact VDFN 8-pin PDIP

2.2 The following table is pin comparison

Pin number	EN25P80	EN25Q80A
Pin1	CS#	CS#
Pin2	DO	DO(DQ1)
Pin3	WP#	WP#(DQ2)
Pin4	VSS	VSS
Pin5	DI	DI(DQ0)
Pin6	CLK	CLK
Pin7	HOLD#	NC(DQ3)
Pin8	VCC	VCC

Note:

If customers don't use Hold# pin function on EN25P80, which can be replaced by EN25Q80A in [standard SPI mode](#).

EN25P80 only support general standard SPI mode.



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EN25Q80A can support general standard / dual / quad SPI mode. (Need specific SPI controller)

2.3 The following tables are the different definitions of block protect area (BP0~BP2)

EN25P80

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Sectors	Addresses	Density(KB)	Portion
1	1	1	All	000000h-0FFFFFFh	1024KB	All
1	1	0	All	000000h-0FFFFFFh	1024KB	All
1	0	1	All	000000h-0FFFFFFh	1024KB	All
1	0	0	Sector 8 to 15	080000h-0FFFFFFh	512KB	Upper 1/2
0	1	1	Sector 12 to 15	0C0000h-0FFFFFFh	256KB	Upper 1/4
0	1	0	Sector 14 to 15	0E0000h-0FFFFFFh	128KB	Upper 1/8
0	0	1	Sector 15	0F0000h-0FFFFFFh	64KB	Upper 1/16
0	0	0	None	None	None	None

EN25Q80A

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 253	000000h-0FDFFFh	1016KB	Lower 127/128
0	1	0	Sector 0 to 251	000000h-0FBFFFh	1008KB	Lower 63/64
0	1	1	Sector 0 to 247	000000h-0F7FFFh	992KB	Lower 31/32
1	0	0	Sector 0 to 239	000000h-0EFFFFh	960KB	Lower 15/16
1	0	1	Sector 0 to 223	000000h-0DFFFFh	896KB	Lower 7/8
1	1	0	Sector 0 to 191	000000h-0BFFFFh	768KB	Lower 3/4
1	1	1	All	000000h-0FFFFFFh	1024KB	All

2.4 For dual output fast read, dual I/O fast read, EQIO, RSTQIO and quad I/O fast read commands and Enter OTP command (3Ah) are only available on EN25Q80A



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q80A (100MHz)		EN25P80 (75MHz)		Unit
	Typ	Max	Typ	Max	
Read I _{CC1}	N/A	25	N/A	20	mA
Write I _{CC2}	N/A	18	N/A	15	mA
Standby I _{CC3}	N/A	5	N/A	20	μA

4. SOFTWARE CONSIDERATIONS

Except of memory type, there is no difference in Manufacture ID, Device ID

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density)

For EN25P80

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	2014h	

For EN25Q80A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	3014h	



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q80A		EN25P80		Unit
	Typ	Max	Typ	Max	
Sector Erase Time	0.09	0.3	0.8	2	Sec
Block Erase Time	0.4	2	N/A	N/A	Sec
Chip Erase Time	5	20	10	20	Sec
Page Programming Time	1.3	5	1.5	5	ms

Note:

N/A means that such parameter is not described and defined in EN25P80 datasheet.

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q80A	EN25P80
tCH (serial clock high time)	Min@ 4ns	Min@ 6ns
tCL (serial clock low time)	Min@ 4ns	Min@ 6ns
tCLCH(serial clock rise time)	Min@ 0.1V / ns	Min@ 0.1V / ns
tCLCL(serial clock fall time)	Min@ 0.1V / ns	Min@ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min@ 5ns	Min@ 5ns
tSHSL(CS# high time)	Min@100ns	Min@100ns
tDSU(Data in setup time)	Min@2ns	Min@2ns
tDH(Data in hold time)	Min@5ns	Min@5ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2009/7/08