



Application Note

EON EN25Q80A

VS

Winbond W25X80A

Specification Comparison



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from Winbond W25X80A Flash to Eon EN25Q80A Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q80A	W25X80A
Voltage Range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin Compatible (Quad mode)	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	8-pin SOP 150mil / 208mil 8-Pad WSON (5x6mm) 8-Pin DIP
SPI frequency (standard / dual / quad mode)	100MHz (standard mode) 80MHz @ dual & quad mode	100MHz @ standard & dual mode
Secured Silicon Sector Region	256 Byte	No
Sector Architecture	Uniform 256 Sectors of 4 K byte 16 blocks of 64 K byte	Uniform Sectors of 4 K byte Blocks of 64 K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
Minimum Endurance Cycle	100K	100K
Package	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	8-pin SOP 150mil / 208mil 8-Pad WSON (5x6mm) 8-Pin DIP



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q80A	W25X80A	Unit
	Max	Max	
Read I _{CC3}	25 @ 100MHz 20 @ 80MHz	18 @ 100MHz 16.5 @ 75MHZ	mA
Page Program (PP) I _{CC4}	28	25	mA
Sector Erase (SE) I _{CC6} Block Erase (BE) I _{CC7}	25	25	mA
Standby I _{CC1}	5	50	μA

3.2 Pin Configuration

Pin number	EN25Q80A	W25X80A
Pin1	CS#	CS#
Pin2	DO (DQ1)	DO
Pin3	WP# (DQ2)	WP#
Pin4	VSS	VSS
Pin5	DI (DQ0)	DIO
Pin6	CLK	CLK
Pin7	NC (DQ3)	Hold
Pin8	VCC	VCC

Note:

1. If customers don't use Hold# pin function on W25X80AV, which can be replaced by EN25Q80A in [standard](#) / [dual SPI mode](#).
2. W25X80A can support general [standard](#) / [dual SPI mode](#).
3. EN25Q80A can support general [standard](#) / [dual](#) / [quad SPI mode](#).
(Need specific SPI controller)



4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

For EN25Q80A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	3014h	

For W25X80A

MANUFACTURER ID	(M7-M0)	
Winbond Serial Flash	EFh	
Device ID	(ID7-ID0)	(ID15-ID0)
Instruction	ABh, 90h	9Fh
W25X80A	13h	3014h



4.2. Instruction Set Comparison

4.2.1 Different Read Status Register content

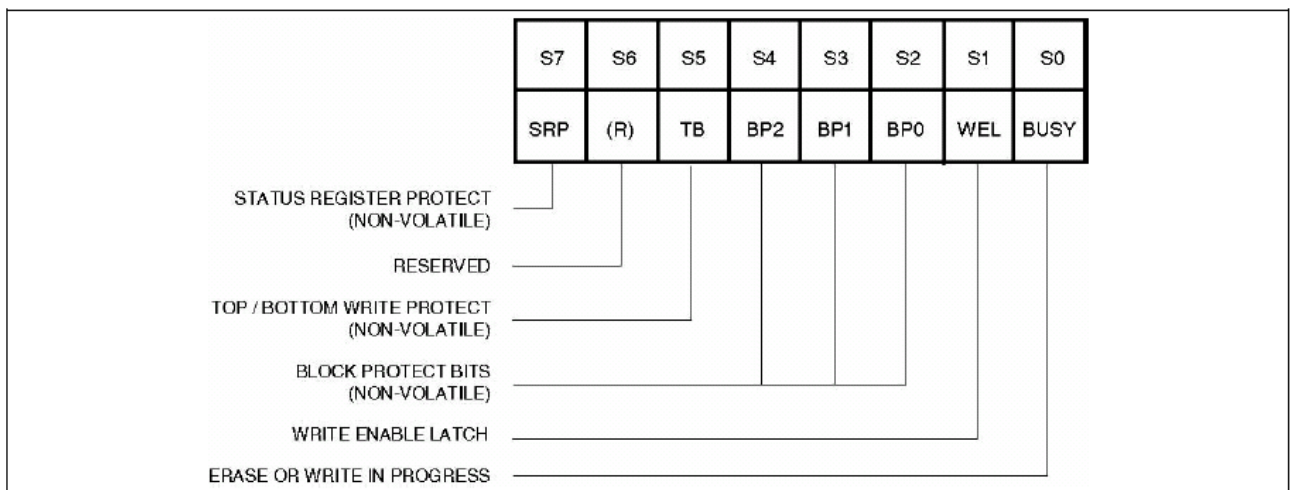
EN25Q80A :

S5 is reserved bit, S6 is WPDIS bit, S7 are SRP bit and OTP_LOCK bit (in OTP mode).

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

W25X80A :

S5 is TB bit, S6 is reserved bit and S7 only is SRP bit.





4.2.2 Different block protect area definitions of (BP0~BP2)

EN25Q80A :

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 253	000000h-0FDFFFh	1016KB	Lower 254/256
0	1	0	Sector 0 to 251	000000h-0FBFFFh	1008KB	Lower 252/256
0	1	1	Sector 0 to 247	000000h-0F7FFFh	992KB	Lower 248/256
1	0	0	Sector 0 to 239	000000h-0EFFFFh	960KB	Lower 240/256
1	0	1	Sector 0 to 223	000000h-0DFFFFh	896KB	Lower 224/256
1	1	0	Sector 0 to 191	000000h-0BFFFFh	768KB	Lower 192/256
1	1	1	All	000000h-0FFFFFFh	1024KB	All

W25X80A :

STATUS REGISTER ⁽¹⁾				W25X80A (8M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	1	15	0F0000h - 0FFFFFFh	64KB	Upper 1/16
0	0	1	0	14 and 15	0E0000h - 0FFFFFFh	128KB	Upper 1/8
0	0	1	1	12 thru 15	0C0000h - 0FFFFFFh	256KB	Upper 1/4
0	1	0	0	8 thru 15	080000h - 0FFFFFFh	512KB	Upper 1/2
1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/16
1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/8
1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/4
1	1	0	0	0 thru 7	000000h - 07FFFFh	512KB	Lower 1/2
x	1	0	1	0 thru 15	000000h - 0FFFFFFh	1MB	ALL
x	1	1	x	0 thru 15	000000h - 0FFFFFFh	1MB	ALL

4.2.3 Enable Quad I/O (EQIO) (38h) command

EN25Q80A : Support.

W25X80A : No support.

4.2.4 Reset Quad I/O (RSTQIO) (FFh) command

EN25Q80A : Support.

W25X80A : No support.



4.2.5 Dual Input / Output FAST_READ (BBh) commands

EN25Q80A : Support.

W25X80A : No support.

4.2.6 Quad Input / Output FAST_READ (EBh) commands

EN25Q80A : Support.

W25X80A : No support.

4.2.7 Enter OTP Mode (3Ah) commands

EN25Q80A : Support.

OTP Sector Address

Sector	Sector Size	Address Range
255	256 byte	0FF000h – 0FF0FFh

Note: The OTP sector is mapping to sector 255

W25X80A : No support.



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q80A		W25X80A		Unit
	Typ	Max	Typ	Max	
Page Programming Time	1.3	5	1.5	3	ms
4 KB Sector Erase Time	0.09	0.3	0.12	0.25	sec
64KB Block Erase Time	0.5	2	0.4	1	sec
Chip (Bulk) Erase Time	8	20	6	10	sec

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q80A	W25X80A
tCH (serial clock high time)	Min @ 4ns	Min @ 4.5ns
tCL (serial clock low time)	Min @ 4ns	Min @ 4.5ns
tCLCH(serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCLCL(serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min @ 5ns	Min @ 5ns
tSHSL(CS# high time)	Min @ 15ns for Read Min @ 50ns for Write	Min @ 50ns for Read Min @ 100ns for Write
tDSU(Data in setup time)	Min @ 2ns	Min @ 2ns
tDH(Data in hold time)	Min @ 5ns	Min @ 5ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2009/9/16