



Migration Note

EON Flash EN25F16 to EN25Q16A



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from EON EN25F16 Flash to Eon EN25Q16A Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table is major features of these two devices.

Features	EN25Q16A	EN25F16
Voltage range	2.7 ~ 3.6	2.7 ~ 3.6
SPI frequency	104MHz (standard mode) 80MHz @ dual & quad mode	100MHz (standard mode)
Secured Silicon Sector region	512 Byte	128 Byte
Sector Architecture	Uniform 512 sectors of 4K byte / 32 block of 64K byte	Uniform 512 sectors of 4K byte / 32 block of 64K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
EQIO mode (Full Quad mode)	Yes	No
Software Reset	Yes	No
Dual Output Fast Read	Yes	No
Dual I/O Fast Read	Yes	No
Quad I/O Fast Read	Yes	No
Page program	Yes	Yes
Sector Erase 4K byte	Yes	Yes
Block (Sector) Erase 64K byte	Yes	Yes
BP table	Enhanced protect (Note)	Conventional
Minimum endurance cycle	100K	100K
Package	8-pin SOP 150mil 8-pin SOP 200mil 8 contact VDFN 8-pin PDIP	8-pin SOP 150mil 8-pin SOP 200mil 8 contact VDFN 8-pin PDIP

Note: Please refer to page 5



2.2 The following table is pin comparison

Pin number	EN25Q16A	EN25F16
Pin1	CS#	CS#
Pin2	DO (DQ1)	DO
Pin3	WP# (DQ2)	WP#
Pin4	VSS	VSS
Pin5	DI (DQ0)	DI
Pin6	CLK	CLK
Pin7	NC (DQ3)	HOLD#
Pin8	VCC	VCC

Note: If customers don't use Hold# pin function on EN25F16, which can be replaced by EN25Q16A in standard SPI mode.

EN25F16 only support general standard SPI mode.

EN25Q16A can support general standard / dual / quad SPI mode. (Need specific SPI controller)

3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q16A	EN25F16	Unit
	Max	Max	
Read I _{CC3}	25	25	mA
Page Program (PP) I _{CC4}	28	28	mA
Sector Erase (SE) I _{CC6}	25	25	mA
Standby I _{CC1}	20	20	μA



4. SOFTWARE CONSIDERATIONS

Except of memory type, (only difference on 9Fh command) there is no difference in Manufacture ID, Device ID

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density)

For EN25Q16A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	3015h	

For EN25F16

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	3115h	



4.2 Instruction Set Comparison

4.2.1 Different Block Protection Area

EN25Q16A :

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 30	000000h-1EFFFFh	1984KB	Lower 31/32
0	0	1	0	Block 0 to 29	000000h-1DFFFFh	1920KB	Lower 30/32
0	0	1	1	Block 0 to 27	000000h-1BFFFFh	1792KB	Lower 28/32
0	1	0	0	Block 0 to 23	000000h-17FFFFh	1536KB	Lower 24/32
0	1	0	1	Block 0 to 15	000000h-0FFFFFFh	1024KB	Lower 16/32
0	1	1	0	All	000000h-1FFFFFFh	2048KB	All
0	1	1	1	All	000000h-1FFFFFFh	2048KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 31 to 1	1FFFFFFh-010000h	1984KB	Upper 31/32
1	0	1	0	Block 31 to 2	1FFFFFFh-020000h	1920KB	Upper 30/32
1	0	1	1	Block 31 to 4	1FFFFFFh-040000h	1792KB	Upper 28/32
1	1	0	0	Block 31 to 8	1FFFFFFh-080000h	1536KB	Upper 24/32
1	1	0	1	Block 31 to 16	1FFFFFFh-100000h	1024KB	Upper 16/32
1	1	1	0	All	1FFFFFFh-000000h	2048KB	All
1	1	1	1	All	1FFFFFFh-000000h	2048KB	All

EN25F16 :

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Block 0 to 30	000000h-1EFFFFh	1984KB	Lower 31/32
0	1	0	Block 0 to 29	000000h-1DFFFFh	1920KB	Lower 30/32
0	1	1	Block 0 to 27	000000h-1BFFFFh	1792KB	Lower 28/32
1	0	0	Block 0 to 23	000000h-17FFFFh	1536KB	Lower 24/32
1	0	1	Block 0 to 15	000000h-0FFFFFFh	1024KB	Lower 16/32
1	1	0	All	000000h-1FFFFFFh	2048KB	All
1	1	1	All	000000h-1FFFFFFh	2048KB	All



4.2.2 Different RDSR bit definition

EN25Q16A :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

EN25F16 :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	Reserved bits	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected			(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit				Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".



4.2.3 Secured OTP Addresses

EN25Q16A :

Sector	Sector Size	Address Range
511	512 byte	1FF000 – 1FF1FFh

Note: The OTP sector is mapping to sector 511

EN25F16 :

Sector	Sector Size	Address Range
511	128 byte	1FF000 – 1FF07Fh

Note: The OTP sector is mapping to sector 511



4.3 Software Reset

There is a new function “Software Reset” in EN25Q16A, which can put the device in normal operating Ready mode.

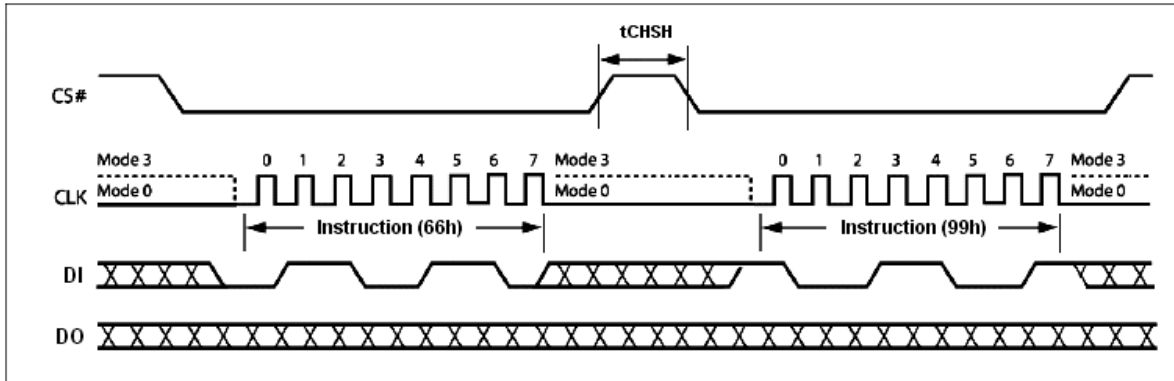


Figure 1. Reset-Enable and Reset Sequence Diagram

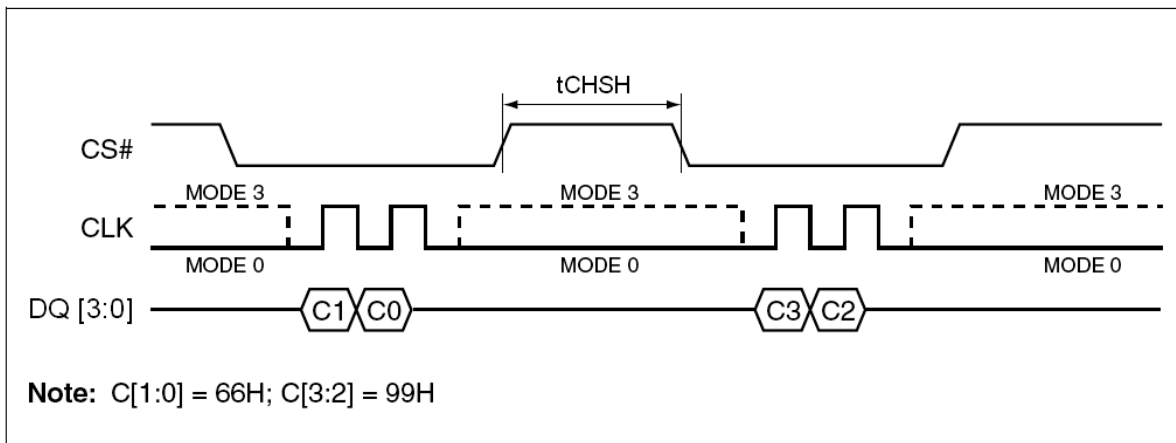


Figure 2 . Reset-Enable and Reset Sequence Diagram under EQIO Mode



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q16A		EN25F16		Unit
	Typ	Max	Typ	Max	
Sector Erase Time	0.05	0.3	0.09	0.3	Sec
Block Erase Time	0.2	2	0.4	2	Sec
Chip Erase Time	6*	12	7*	35	Sec
Page Programming Time	0.8	5	1.3	5	ms

* **NOTE:** ERASE FROM “1” → “1”.

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q16A	EN25F16
tCH (serial clock high time)	Min@ 4ns	Min@ 4ns
tCL (serial clock low time)	Min@ 4ns	Min@ 4ns
tCLCH(serial clock rise time)	Min@ 0.1V / ns	Min@ 0.1V / ns
tCLCL(serial clock fall time)	Min@ 0.1V / ns	Min@ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min@ 5ns	Min@ 5ns
tSHSL(CS# high time)	Min, read @15ns Program/Erase @50ns	Min@100ns
tDSU(Data in setup time)	Min@2ns	Min@2ns
tDH(Data in hold time)	Min@5ns	Min@5ns



Eon Silicon Solution Inc.

Revisions List

Revision No	Description	Date
A	Initial Release	2010/10/14