



Application Note

EON EN25Q40 (Version: D)

VS.

ESMT F25L004A (Version: 1.3)



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from ESMT flash F25L004A to Eon flash EN25Q40.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1. The following table highlights the major features of these two devices.

Features	EN25Q40	F25L004A
Voltage Range	2.7V ~ 3.6V	2.7V(3.3V@100MHz) ~ 3.6V
Pin to Pin Compatible	Yes	Yes
SPI Mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI Frequency	100MHz (standard mode) 80MHz @ dual & quad mode	100MHz (standard mode)
Sector Architecture	Uniform ● 128 sectors of 4Kbyte ● 8 blocks of 64Kbyte ● Any sector or block can be erased individually.	Uniform ● 128 sectors of 4Kbyte ● 8 blocks of 64Kbyte ● Any sector or block can be erased individually.
Lockable OTP Security Sector	256 Bytes	No
Minimum Endurance Cycle	100K	100K
Package ¹ .	8 pins SOP 150mil body width 8 contact VDFN (5x6mm) ● All Pb-free packages are RoHS compliant	8 pins SOP 150mil body width ● All Pb-free packages are RoHS compliant

Note:

1. Please refer to the datasheet in detail.



3. HARDWARE CONSIDERATIONS

3.1. I_{CC} Comparison

Current	EN25Q40	F25L004A	Unit
	Max (@ Single 100MHz)	Max (@ 33MHz)	
Read I _{CC3}	25	15	mA
Page Program (PP) I _{CC4}	28	40	mA
Sector Erase (SE) I _{CC6}	25	40	mA
Standby I _{CC1}	20	75	μA

3.2. Pins Description

EN25Q40		F25L004A	
Pin Name	Function	Pin Name	Function
CLK	Serial Clock Input	SCK	Serial Clock Input
DI (DQ0)	Serial Data Input (Data Input Output 0) *1	SI	Serial Data Input
DO (DQ1)	Serial Data Output (Data Input Output 1) *1	SO	Serial Data Output
CS#	Chip Enable	CS#	Chip Enable
WP# (DQ2)	Write Protect (Data Input Output 2) *2	WP#	Write Protect
NC(DQ3)	Not Connect (Data Input Output 3) *2	HOLD#	Hold Input
V _{CC}	Supply Voltage (2.7-3.6V)	VDD	Supply Voltage (2.7-3.6V)
V _{SS}	Ground	V _{SS}	Ground
NC	No Connect	NC	No Connect

Note:

1. DQ0 and DQ1 are used for Dual and Quad instructions.
2. DQ0 ~ DQ3 are used for Quad instructions.

* Users must take care of the different pin definition!



4. SOFTWARE CONSIDERATIONS

4.1. Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

4.1.1. For **EN25Q40** : MANUFACTURER/DEVICE ID TABLE

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			12h
90h	1Ch		12h
9Fh	1Ch	3013h	

4.1.2. For **F25L004A** : MANUFACTURER/DEVICE ID TABLE

JEDEC READ-ID DATA

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
8CH	20H	13H



4.2. Instruction Set Comparison

4.2.1. For **EN25Q40** : Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQIO	38h						
RSTQIO ⁽¹⁾	FFh						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0) ⁽²⁾					continuous ⁽³⁾
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(4)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(5)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(6)		
Enter OTP mode	3Ah						

Notes:

1. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode
2. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “ () ” indicate data being read from the device on the DO pin.
3. The Status Register contents will repeat continuously until CS# terminates the instruction.
4. The Device ID will repeat continuously until CS# terminates the instruction.
5. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
6. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.



Instruction Set (Read Instruction)

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) ⁽¹⁾	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8 ⁽²⁾	A7-A0, dummy ⁽²⁾	(D7-D0, ...) ⁽¹⁾			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh	A23-A0, dummy ⁽⁴⁾	(dummy, D7-D0) ⁽⁵⁾	(D7-D0, ...) ⁽³⁾			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data

$$DQ_0 = (D6, D4, D2, D0)$$

$$DQ_1 = (D7, D5, D3, D1)$$

2. Dual Input Address

$$DQ0 = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, \text{dummy } 6, \text{dummy } 4, \text{dummy } 2, \text{dummy } 0$$

$$DQ1 = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, \text{dummy } 7, \text{dummy } 5, \text{dummy } 3, \text{dummy } 1$$

3. Quad Data

$$DQ0 = (D4, D0, \dots)$$

$$DQ1 = (D5, D1, \dots)$$

$$DQ2 = (D6, D2, \dots)$$

$$DQ3 = (D7, D3, \dots)$$

4. Quad Input Address

$$DQ0 = A20, A16, A12, A8, A4, A0, \text{dummy } 4, \text{dummy } 0$$

$$DQ1 = A21, A17, A13, A9, A5, A1, \text{dummy } 5, \text{dummy } 1$$

$$DQ2 = A22, A18, A14, A10, A6, A2, \text{dummy } 6, \text{dummy } 2$$

$$DQ3 = A23, A19, A15, A11, A7, A3, \text{dummy } 7, \text{dummy } 3$$

5. Quad I/O Fast Read Data

$$DQ0 = (\text{dummy } 12, \text{dummy } 8, \text{dummy } 4, \text{dummy } 0, D4, D0)$$

$$DQ1 = (\text{dummy } 13, \text{dummy } 9, \text{dummy } 5, \text{dummy } 1, D5, D1)$$

$$DQ2 = (\text{dummy } 14, \text{dummy } 10, \text{dummy } 6, \text{dummy } 2, D6, D2)$$

$$DQ3 = (\text{dummy } 15, \text{dummy } 11, \text{dummy } 7, \text{dummy } 3, D7, D3)$$



4.2.2. For F25L004A : Instruction Set

DEVICE OPERATION INSTRUCTIONS

Cycle Type/ Operation ^{1,2}	Max Freq	Bus Cycle											
		1		2		3		4		5		6	
		S _{IN}	S _{OUT}	S _{IN}	S _{OUT}	S _{IN}	S _{OUT}	S _{IN}	S _{OUT}	S _{IN}	S _{OUT}	S _{IN}	S _{OUT}
Read	33 MHz	03H	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	X	D _{OUT}		
High-Speed-Read		0BH	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	X	X	X	D _{OUT}
Sector-Erase ^{4,5} (4K Byte)		20H	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	-	-	-	-
Block-Erase ⁵ (64K Byte)		D8H	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	-	-	-	-
Chip-Erase ⁵		60H C7H	Hi-Z	-	-	-	-	-	-	-	-	-	-
Byte-Program ⁵		02H	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	D _{IN}	Hi-Z	-	-
Auto-Address-Increment-word programming (AAI) ⁶		ADH	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	D _{IN0}	Hi-Z	D _{IN1}	Hi-Z
Read-Status-Register (RDSR)	50MHz	05H	Hi-Z	X	D _{OUT}	-	Note ⁷	-	Note ⁷	-	Note ⁷	-	-
Enable-Write-Status-Register (EWSR) ⁸		50H	Hi-Z	-	-	-	-	-	-	-	-	-	-
Write-Status-Register (WRSR) ⁸		01H	Hi-Z	Data	Hi-Z	-	-	-	-	-	-	-	-
Write-Enable (WREN) ¹¹		06H	Hi-Z	-	-	-	-	-	-	-	-	-	-
Write-Disable (WRDI)		04H	Hi-Z	-	-	-	-	-	-	-	-	-	-
Read-Electronic-Signature ⁹ (RES)	100MHz	ABH	Hi-Z	X	12H	-	-	-	-	-	-	-	-
Jedec-Read-ID (JEDEC-ID) ¹⁰		9FH	Hi-Z	X	8CH	X	20H	X	13H	-	-	-	-
Read-ID (RDID)		90H (A0=0)	Hi-Z	A ₂₃ -A ₁₆	Hi-Z	A ₁₅ -A ₈	Hi-Z	A ₇ -A ₀	Hi-Z	X	8CH	X	12H
		90H (A0=1)									12H		8CH
Enable SO to output RY/BY# Status during AAI (EBSY)		70H	Hi-Z	-	-	-	-	-	-	-	-	-	-
Disable SO to output RY/BY# Status during AAI (DBSY)		80H	Hi-Z	-	-	-	-	-	-	-	-	-	-

1. Operation: S_{IN} = Serial In, S_{OUT} = Serial Out
2. X = Dummy Input Cycles (V_{IL} or V_{IH}); - = Non-Applicable Cycles (Cycles are not necessary)
3. One bus cycle is eight clock periods.
4. Sector addresses: use AMS-A12, remaining addresses can be V_{IL} or V_{IH}
5. Prior to any Byte-Program, Sector-Erase, Block-Erase, or Chip-Erase operation, the Write-Enable (WREN) instruction must be executed.
6. To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by the data to be programmed.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on \overline{CE} .
8. The Enable-Write-Status-Register (EWSR) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the EWSR instruction to make both instructions effective.
9. The Read-Electronic-Signature is continuous with on going clock cycles until terminated by a low to high transition on \overline{CE} .
10. The Jedec-Read-ID is output first byte 8CH as manufacture ID; second byte 20H as top memory type; third byte 13H as memory capacity.
11. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both instructions effective. Both EWSR and WREN can enable WRSR, user just need to execute one of it. A successful WRSR can reset WREN.

Note:

1. The major differences are pointed out by the blue arrows. Please refer to the datasheet in detail.
2. Users must modify the codes for EN25Q40!



4.3. Different Block Protection Area

*The definitions of Block Protection Area are different!

4.3.1. For EN25Q40 :

Protected Area Sizes Sector Organization Table

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 125	000000h-07DFFFh	504KB	Lower 126/128
0	1	0	Sector 0 to 123	000000h-07BFFFh	496KB	Lower 124/128
0	1	1	Sector 0 to 119	000000h-077FFFh	480KB	Lower 120/128
1	0	0	Sector 0 to 111	000000h-06FFFFh	448KB	Lower 112/128
1	0	1	Sector 0 to 95	000000h-05FFFFh	384KB	Lower 096/128
1	1	0	Sector 0 to 63	000000h-03FFFFh	256KB	Lower 064/128
1	1	1	All	000000h-07FFFFh	512KB	All

4.3.2. For F25L004A :

F25L004A Block Protection Table

Protection Level	Status Register Bit			Protected Memory Area	
	BP2	BP1	BP0	Block Range	Address Range
0	0	0	0	None	None
Upper 1/8	0	0	1	Block 7	70000H – 7FFFFH
Upper 1/4	0	1	0	Block 6~7	60000H – 7FFFFH
Upper 1/2	0	1	1	Block 4~7	40000H – 7FFFFH
All Blocks	1	0	0	Block 0~7	00000H – 7FFFFH
All Blocks	1	0	1	Block 0~7	00000H – 7FFFFH
All Blocks	1	1	0	Block 0~7	00000H – 7FFFFH
All Blocks	1	1	1	Block 0~7	00000H – 7FFFFH



4.4. Different RDSR Bits Definition

*The definitions of RDSR bits [S7:S6] are different!

4.4.1. For EN25Q40 :

Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

4.4.2. For F25L004A :

SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 2)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 2)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 2)	1	R/W
5	RESERVED	Reserved for future use	0	N/A
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP2,BP1,BP0 are read-only bits 0 = BP2,BP1,BP0 are read/writable	0	R/W

Note1 : Only BP0,BP1,BP2 and BPL are writable

Note2 : All register bits are volatility

Note3 : All area are protected at power-on (BP2=BP1=BP0=1)



4.5. Different One Time Programming Definition

*The definitions of OTP are different!

4.5.1. For EN25Q40 :

OTP Sector Address

Sector	Sector Size	Address Range
127	256 byte	07F000h – 07F0FFh

Note: The OTP sector is mapping to sector 127

4.5.2. For F25L004A : NO



5. PERFORMANCE DIFFERENCES

5.1. KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q40	F25L004A
t _{CH} (serial clock high time)	Min @ 4ns	Min @ 5ns
t _{CL} (serial clock low time)	Min @ 4ns	Min @ 5ns
t _{CLCH} (serial clock rise time)	Min @ 0.1V / ns	
t _{CLCL} (serial clock fall time)	Min @ 0.1V / ns	
t _{CHSH} (CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
t _{SHSL} (CS# high time)	Min @ 100ns	Min @ 100ns
t _{DSU} (Data in setup time)	Min @ 2ns	Min @ 3ns
t _{DH} (Data in hold time)	Min @ 5ns	Min @ 3ns

5.2. Power-On Timings

Parameter	Description	EN25Q40	F25L004A
t _{VSL}	V _{CC} (min) to CS# low	10μs	10μs
t _{PUW}	Time delay to Write instruction	10ms	

5.3. ERASE AND PROGRAM PERFORMANCE

The ERASE and PROGRAM Performance Comparison

Parameter	EN25Q40		F25L004A		Unit
	Typ	Max	Typ	Max	
Page programming time	1.3ms	5ms	9μs* ¹	300μs* ¹	
Sector erase time	0.09	0.3	0.09	0.2	sec
Block erase time	0.5	2	1	2	sec
Chip (Bulk) erase time	3.5	10	12	100	sec

Note:

1. For one byte programming time.



Eon Silicon Solution Inc.

Revisions List

Revision No	Description	Date
A	Initial Release	2010/11/3