



## **Application Note**

**EON**                      **EN29LV320B**                      (Version: C)  
**VS.**  
**Atmel**                      **AT49BV322D**                      (Version: B)



# Eon Silicon Solution Inc.

## 1. INTRODUCTION

The application note introduces how to implement a system design from Atmel flash AT49BV322D to Eon flash EN29LV320B.

## 2. GENERAL FUNCTION COMPARISON TABLE:

2.1. The following table is major features of these two devices.

Features	EN29LV320B	AT49BV322D
Voltage Range	2.7V ~ 3.6V	2.65V ~ 3.6V
Pin to Pin <sup>1</sup> .	YES	YES
Access Time	70ns	70ns
Sector Architecture	Sector of 4KWord/8Kbyte x8 (Top or Bottom Location) Sector of 32KWord/64Kbyte x63	Sector of 4KWord/8Kbyte x8 (Top or Bottom Location) Sector of 32KWord/64Kbyte x63
Secured Silicon Sector	NO	128 Bits
Byte/Word Mode	Yes	Yes
WP# / ACC Pin	<ul style="list-style-type: none"><li>● Write protect (WP#) function: Yes</li><li>● Acceleration (ACC) function: Yes</li></ul>	<ul style="list-style-type: none"><li>● Write protect (WP#) function: Yes</li><li>● Acceleration (ACC) function: Yes</li></ul>
Sector Protection	Yes	Yes
Data# Polling and Toggle Bits	Yes	Yes
V <sub>ID</sub> and V <sub>HH</sub> Range	10.5V – 11.5V	9V – 10V
Erase Suspend/Resume	Yes	Yes
Program Suspend/Resume	No	Yes
CFI Compliant	Yes	Yes
Minimum Endurance Cycle	100K	100K
Package <sup>1</sup> .	48-pin TSOP (Type 1) 48-ball 6mm x 8mm TFBGA	48-pin TSOP 48-ball 6mm x 8mm TFBGA

### Note:

1. Please refer to the datasheet in detail.



## 3. HARDWARE CONSIDERATIONS

### 3.1. I<sub>CC</sub> Comparison

Current	EN29LV320B		AT49BV322D		Unit
	Typ	Max	Typ	Max	
Read I <sub>CC1</sub>	9	16 <sup>1</sup>	10	15 <sup>1</sup>	mA
Write I <sub>CC2</sub>	20	30		25	mA
Standby I <sub>CC3</sub>	1	5.0	15	25	μA

Note :

- f=5MHz

### 3.2. Pins Description

EN29LV320B		AT49BV322D	
Pin Name	Function	Pin Name	Function
A0-A20	21 Address inputs	A0-A20	21 Address inputs
DQ0-DQ14	15 Data Inputs/Outputs	I/O0-I/O14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)	I/O15 (A-1)	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable	CE#	Chip Enable
OE#	Output Enable	OE#	Output Enable
WE#	Write Enable	WE#	Write Enable
WP# / ACC <sup>1</sup>	Write Protect / Acceleration Pin	V <sub>PP</sub>	Acceleration Pin / Write Protect
RESET# <sup>2</sup>	Hardware Reset Pin	RESET#	Hardware Reset Pin / Block Temporary Unprotect
BYTE#	Byte/Word Mode Selection	BYTE#	Byte/Word Mode Selection
RY/BY#	Ready/Busy Output	RDY/BUSY#	Ready/Busy Output
V <sub>CC</sub>	Supply Voltage (2.7-3.6V)	V <sub>CC</sub>	Supply Voltage (2.7-3.6V)
V <sub>SS</sub>	Ground	V <sub>SS</sub>	Ground
NC	Not Connected to anything	NC	Not Connected to anything

Note :

- The WP#/ACC pin must not be left floating or unconnected.
- Also support temporary sector unprotect function when REST#=V<sub>ID</sub>.

\* Users must take care of the different pin definition!



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## 4. Autoselect Codes (Using High Voltage, $V_{ID}$ )

### 4.1. For EN29LV320B : 32M FLASH MANUFACTURER/DEVICE ID TABLE

Description		CE#	OE#	WE#	A20 to A12	A11 to A10	A9 <sup>2</sup>	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Eon		L	L	H	X	X	$V_{ID}$	H <sup>1</sup>	X	L	X	L	L	X	1Ch
								L							7Fh
Device ID (top boot sector)	Word	L	L	H	X	X	$V_{ID}$	X	X	L	X	L	H	22h	F6h
	Byte	L	L	H										X	F6h
Device ID (bottom boot sector)	Word	L	L	H	X	X	$V_{ID}$	X	X	L	X	L	H	22h	F9h
	Byte	L	L	H										X	F9h
Sector Protection Verification		L	L	H	SA	X	$V_{ID}$	X	X	L	X	H	L	X	01h (Protected)
														X	00h (Unprotected)

L=logic low=  $V_{IL}$ , H=Logic High=  $V_{IH}$ ,  $V_{ID} = 9 \pm 0.5V$ , X=Don't Care (either L or H, but not floating!), SA=Sector Addresses

**Note:**

1. A8 = H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 =  $V_{ID}$  is for HV A9 Autoselect mode only. A9 must be  $\leq V_{CC}$  (CMOS logic level) for Command Autoselect Mode.



## 4.2. For AT49BV322D : MANUFACTURER/DEVICE ID TABLE

Mode	CE	OE	WE	RESET	V <sub>PP</sub> <sup>(1)</sup>	Ai	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X <sup>(2)</sup>	Ai	D <sub>OUT</sub>
Program/Erase <sup>(3)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IHPP</sub> <sup>(4)</sup>	Ai	D <sub>IN</sub>
Standby/Program Inhibit	V <sub>IH</sub>	X <sup>(2)</sup>	X	V <sub>IH</sub>	X	X	High-Z
Program Inhibit	X	X	V <sub>IH</sub>	V <sub>IH</sub>	X		
	X	V <sub>IL</sub>	X	V <sub>IH</sub>	X		
	X	X	X	V <sub>IH</sub>	V <sub>ILPP</sub> <sup>(5)</sup>		
Output Disable	X	V <sub>IH</sub>	X	V <sub>IH</sub>	X		High-Z
Reset	X	X	X	V <sub>IL</sub>	X	X	High-Z
Product Identification Software <sup>(6)</sup>				V <sub>IH</sub>		A0 = V <sub>IL</sub> , A1 - A20 = V <sub>IL</sub>	Manufacturer Code <sup>(7)</sup>
						A0 = V <sub>IH</sub> , A1 - A20 = V <sub>IL</sub>	Device Code <sup>(7)</sup>

- Notes:
1. The VPP pin can be tied to V<sub>CC</sub>. For faster program operations, V<sub>PP</sub> can be set to 9.5V ± 0.5V.
  2. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  3. Refer to "Program Cycle Waveforms" on page 24.
  4. V<sub>IHPP</sub> (min) = 1.65V
  5. V<sub>ILPP</sub> (max) = 0.4V.
  6. See details under "Software Product Identification Entry/Exit" on page 26.
  7. Manufacturer Code: 1FH (x8); 001FH (x16), Device Code: C8H (x8) - AT49BV322D; 01C8H (x16) - AT49BV322D; C9H (x8) - AT49BV322DT; 01C9H (x16) - AT49BV322DT.



## 5. SOFTWARE CONSIDERATIONS

### 5.1. SECURED SILICON SECTOR

#### 5.1.1. For EN29LV320B : NO

#### 5.1.2. For AT49BV322D : 128 Bits

**Protection Register Addressing Table<sup>(1)(2)(3)</sup>**

Address	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
81	Factory	A	1	0	0	0	0	0	0	1
82	Factory	A	1	0	0	0	0	0	1	0
83	Factory	A	1	0	0	0	0	0	1	1
84	Factory	A	1	0	0	0	0	1	0	0
85	User	B	1	0	0	0	0	1	0	1
86	User	B	1	0	0	0	0	1	1	0
87	User	B	1	0	0	0	0	1	1	1
88	User	B	1	0	0	0	1	0	0	0

- Notes:
1. All address lines not specified in the above table must be "0" when accessing the protection register, i.e., A20 - A8 = 0.
  2. The addressing shown above should be used when the device is operating in the word (x16) mode.
  3. In the byte (x8) mode, A-1 should be used when addressing the protection register:
    - with A-1 = 0, the LSB of the address location can be accessed; and
    - with A-1 = 1, the MSB of the address location can be accessed



## 5.2. COMMANDS DEFINITION

### 5.2.1. For EN29LV320B :

Command Sequence			Cycles	Bus Cycles											
				1 <sup>st</sup> Cycle		2 <sup>nd</sup> Cycle		3 <sup>rd</sup> Cycle		4 <sup>th</sup> Cycle		5 <sup>th</sup> Cycle		6 <sup>th</sup> Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
		Byte		AAA		555		AAA		100	1C				
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	x01	22F6				
		Byte		AAA		555		AAA		000	7F				
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	x01	22F9				
		Byte		AAA		555		AAA		200	1C				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA)	00				
		Byte		AAA		555		AAA		X02	01				
Program			4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Chip Erase			6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA	555	AAA			
Sector Erase			6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA	555	AAA			
Sector Erase Suspend			1	XXX	B0										
Sector Erase Resume			1	XXX	30										
CFI Query			1	55	98										
		Byte		AA											

Address and Data values indicated are in hex. Unless specified, all bus cycles are write cycles

RA = Read Address: address of the memory location to be read. This is a read cycle.

RD = Read Data: data read from location RA during Read operation. This is a read cycle.

PA = Program Address: address of the memory location to be programmed. X = Don't-Care

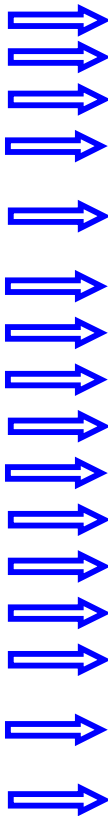
PD = Program Data: data to be programmed at location PA

SA = Sector Address: address of the Sector to be erased or verified. Address bits A20-A12 uniquely select any Sector.



## 5.2.2. For AT49BV322D :

### Command Definition Table



Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D <sub>OUT</sub>										
Chip Erase	6	555	AA	AAA <sup>(2)</sup>	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA <sup>(3)</sup>	30
Byte/Word Program	4	555	AA	AAA	55	555	A0	Addr	D <sub>IN</sub>				
Dual Byte/Word Program <sup>(4)</sup>	5	555	AA	AAA	55	555	E0	Addr0	D <sub>IN0</sub>	Addr1	D <sub>IN1</sub>		
Enter Single Pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single Pulse Byte/Word Program	1	Addr	D <sub>IN</sub>										
Sector Lockdown	6	555	AA	AAA <sup>(2)</sup>	55	555	80	555	AA	AAA	55	SA <sup>(3)(5)</sup>	60
Erase/Program Suspend	1	XXX	B0										
Erase/Program Resume	1	XXX	30										
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit <sup>(6)</sup>	3	555	AA	AAA	55	555	F0 <sup>(7)</sup>						
Product ID Exit <sup>(6)</sup>	1	XXX	F0 <sup>(7)</sup>										
Program Protection Register	4	555	AA	AAA	55	555	C0	Addr <sup>(8)</sup>	D <sub>IN</sub>				
Lock Protection Register - Block B	4	555	AA	AAA	55	555	C0	080	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	80	D <sub>OUT</sub> <sup>(9)</sup>				
Set Configuration Register	4	555	AA	AAA	55	555	D0	XXX	00/01 <sup>(10)</sup>				
CFI Query <sup>(11)</sup>	1	X55	98										

- Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A20 through A11 are don't care in the word mode. Address A20 through A11 and A-1 are don't care in the byte mode.
  2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
  3. SA = sector address. Any byte/word address within a sector can be used to designate the sector address (see pages 15 - 18 for details).
  4. This fast programming option enables the user to program two words in parallel only when V<sub>PP</sub> = 9.5V. The Addresses, Addr0 and Addr1, of the two words, D<sub>IN0</sub> and D<sub>IN1</sub>, must only differ in address A0. This command should be used during manufacturing purposes only.
  5. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
  6. Either one of the Product ID Exit commands can be used.
  7. Bytes of data other than F0 may be used to exit the Product ID mode. However, it is recommended that F0 be used.
  8. Any addresses within the user programmable protection register region. Address locations are shown on "Protection Register Addressing Table<sup>(1)(2)(3)" on page 14.</sup>
  9. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
  10. The default state (after power-up) of the configuration register is "00".
  11. When accessing the data in the CFI table, the address format is A15 - A0 (Hex) in the word mode and A14 - A1 (Hex) in the byte mode.

### Note:

1. The major differences are pointed out by the blue arrows. Please refer to the datasheet in detail.
2. Users must modify the codes for EN29LV320B.



## 6. WRITE OPERATION STATUS

### 6.1. For EN29LV320B :

Operation		DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A	0

### Status Register Bits

DQ	Name	Logic Level	Definition
7	DATA# POLLING	'1'	Erase Complete or erased sector in Sector Erase Suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erased sector during Sector Erase Suspend
		DQ7#	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Sector Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	TIME OUT BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	ERASE TIME OUT BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Sector Erase or Read within Erase-Suspended sector. (When DQ5=1, Erase Error due to currently addressed Sector or Program on Erase-Suspended sector)
		DQ2	Read on addresses of non Erase-Suspend sectors



## Notes:

### **DQ7: DATA# Polling:**

Indicates the P/E status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

### **DQ6: Toggle Bit:**

Remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

### **DQ5: Time Out Bit:**

Set to "1" if failure in programming or erase

### **DQ3: Sector Erase Command Timeout Bit:**

Operation has started. Only possible command is Erase suspend (ES).

### **DQ2: Toggle Bit:**

Indicates the Erase status and allows identification of the erased Sector.



## 6.2. For AT49BV322D :

### Status Bit Table

Configuration Register	Status Bit						
	I/O7	I/O7	I/O6	I/O5 <sup>(1)</sup>	I/O3 <sup>(2)</sup>	I/O2	RDY/BUSY
	00	01	00/01	00/01	00/01	00/01	00/01
Programming	$\overline{I/O7}$	0	TOGGLE	0	0	1	0
Erasing	0	0	TOGGLE	0	0	TOGGLE	0
Erase Suspended & Read Erasing Sector	1	1	1	0	0	TOGGLE	1
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA	1
Erase Suspended & Program Non-erasing Sector	$\overline{I/O7}$	0	TOGGLE	0	0	TOGGLE	0
Erase Suspended & Program Suspended and Reading from Non-suspended Sectors	DATA	DATA	DATA	DATA	DATA	DATA	1
Program Suspended & Read Programming Sector	I/O7	1	1	0	0	TOGGLE	1
Program Suspended & Read Non-programming Sector	DATA	DATA	DATA	DATA	DATA	DATA	1

- Notes:
1. I/O5 switches to a "1" when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.
  2. I/O3 switches to a "1" when the  $V_{PP}$  level is not high enough to successfully perform program and erase operations.



## 7. PERFORMANCE DIFFERENCES

### 7.1. Power-On and Hardware Reset (RESET#) Timings

Parameter	Description	EN29LV320B	AT49BV322D
t <sub>VCS</sub>	Vcc Setup Time	50μs	
t <sub>RP1</sub>	RESET# Pulse Width (During Embedded Algorithms)	10μs	
t <sub>RP2</sub>	RESET# Pulse Width (NOT During Embedded Algorithms)	500ns	500ns
t <sub>RH</sub>	Reset# High Time Before Read	50ns	100ns
t <sub>RB1</sub>	RY/BY# Recovery Time ( to CE#, OE# go low)	0ns	
t <sub>RB2</sub>	RY/BY# Recovery Time ( to WE# go low)	50ns	
t <sub>READY1</sub>	Reset# Pin Low (During Embedded Algorithms) to Read or Write	20μs	
t <sub>READY2</sub>	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	500ns	

### 7.2. ERASE AND PROGRAM PERFORMANCE

#### The ERASE and PROGRAM Performance Comparison

Parameter	EN29LV320B		AT49BV322D		Unit
	Typ	Max	Typ	Max	
Sector Erase Time	0.1	2	0.5	6	sec
Chip Erase Time	8	70		33	sec
Byte Programming Time	8	200	10	120	μs
Word Programming Time	8	200	10	120	μs
Accelerated Byte/Word Program Time	7	200			μs
Chip Programming Time	Byte	33.6	100.8		sec
	Word	16.8	50.4		sec
Erase/Program Endurance	100K		100K		Cycles

**Notes:**

1. Typical program and erase times assume the following conditions: room temperature, 3V and checkerboard pattern programmed.
2. Maximum program and erase times assume the following conditions: worst case Vcc, 90°C and 100,000 cycles.



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## Revisions List

Revision No	Description	Date
A	Initial Release	2010/10/26