



Application Note

EON EN25Q32A

VS

Atmel AT25DF321A

Specification Comparison



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from Atmel AT25DF321A Flash to Eon EN25Q32A Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q32A	AT25DF321A
Voltage Range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin Compatible (standard SPI mode)	8-pins SOP 200mil Except pin 7 = NC 8-pins VDFN (5mm x 6mm) Except pin 7 = NC and Thickness A = 0.75mm (normal)	8S2 – EIAJ SOIC Except pin 7 = HOLD# 8MA1 – UDFN (5mm x 6mm) Except pin 7 = HOLD# and Thickness A = 0.55mm (normal)
SPI frequency	100MHz (standard mode) 80MHz @ dual & quad mode	100MHz (for RapidS) 85MHz for SPI
Secured Silicon Sector Region	512 Byte	128 Byte
Sector Architecture	Uniform 1024 sectors of 4K byte 64 blocks of 64K byte	Uniform 1024 sectors of 4K byte 128 blocks of 32K byte 64 blocks of 64K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
EQIO mode (Full Quad mode)	Yes	No
RapidS Operation	No	Yes
Page program	Yes	Yes
Sector erase 4K byte	Yes	Yes
Block erase 32K Byte	No	Yes
Block erase 64K byte	Yes	Yes
Program and Erase Suspend / Resume	No	Yes
Individual Sector Protection with Global Protect / Unprotect	No	Yes
Read Sector Protection Registers	No	Yes
Sector Lockdown	No	Yes
Software Controlled Reset	No	Yes
Minimum Endurance Cycle	100K	100K
Package	16-pins SOP 300mil 8-pins SOP 200mil 8-pins VDFN (5mm x 6mm) 8-pins DIP	8S2 – EIAJ SOIC 8MA1 – UDFN (5mm x 6mm)

Note: For general and dual SPI modes hold# on EN25Q32A is NC.



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q32A	AT25DF321A	Unit
	Max	Max	
Read I _{CC3}	25 @ 100MHz 20 @ 80MHz (dual)	19 @ 100MHz 17 @ 85MHz	mA
Page Program (PP) I _{CC4}	28	15	mA
Sector Erase (SE) I _{CC6}	25	18	mA
Standby I _{CC1}	20	50	μA

3.2 Pin Configuration (8-pin package)

Pin number	EN25Q32A	AT25DF321A
Pin 1	CS#	CS#
Pin 2	DO (DQ1)	SO (SOI)
Pin 3	WP# (DQ2)	WP#
Pin 4	VSS	GND
Pin 5	DI (DQ0)	SI (SIO)
Pin 6	CLK	SCK
Pin 7	NC (DQ3)	HOLD#
Pin 8	VCC	VCC

Note:

1. If customers don't use Hold# pin function on AT25DF321A, which can be replaced by EN25Q32A in standard SPI mode.
2. Eon EN25Q32A Flash can support the general standard / dual / quad SPI mode (Need specific SPI controller).
3. For general and dual SPI modes, Eon EN25Q32A Flash is the same as Atmel AT25DF321A Flash if customer don't use the HOLD# pin function.
4. Atmel AT25DF321A doesn't support quad SPI mode.
5. If customers will use the VDFN (UDFN) package, please take care the dimensions of thickness "A".

Part No	EN35Q32A (8 -VDFN)			AT25DF321A (8-UDFN)		
	DIMENSION IN MM			DIMENSION IN MM		
SYMBOL	MIN.	NOR	MAX	MIN.	NOR	MAX
A	0.7	0.75	0.8	0.45	0.55	0.6



4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

For EN25Q32A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			15h
90h	1Ch		15h
9Fh	1Ch	3016h	

For AT25DF321A

Byte No.	Data Type	Value
1	Manufacturer ID	1Fh
2	Device ID (Part 1)	47h
3	Device ID (Part 2)	01h
4	Extended Device Information String Length	00h

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1Fh	JEDEC Code: 0001 1111 (1Fh for Atmel)
	0	0	0	1	1	1	1	1		
Device ID (Part 1)	Family Code			Density Code					47h	Family Code: 010 (AT25DF/26DFxxx series) Density Code: 00111 (32-Mbit)
	0	1	0	0	0	1	1	1		
Device ID (Part 2)	Sub Code			Product Version Code					01h	Sub Code: 000 (Standard series) Product Version: 00001 (First major revision)
	0	0	0	0	0	0	0	1		



4.2. Instruction Set Comparison

4.2.1 Different Block (Sector) Protection Area

EN25Q32A :

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 62	000000h-3EFFFFh	4032KB	Lower 63/64
0	0	1	0	Block 0 to 61	000000h-3DFFFFh	3968KB	Lower 62/64
0	0	1	1	Block 0 to 59	000000h-3BFFFFh	3840KB	Lower 60/64
0	1	0	0	Block 0 to 55	000000h-37FFFFh	3584KB	Lower 56/64
0	1	0	1	Block 0 to 47	000000h-2FFFFFFh	3072KB	Lower 48/64
0	1	1	0	Block 0 to 31	000000h-1FFFFFFh	2048KB	Lower 32/64
0	1	1	1	All	000000h-3FFFFFFh	4096KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 63 to 1	3FFFFFFh-010000h	4032KB	Upper 63/64
1	0	1	0	Block 63 to 2	3FFFFFFh-020000h	3968KB	Upper 62/64
1	0	1	1	Block 63 to 4	3FFFFFFh-040000h	3840KB	Upper 60/64
1	1	0	0	Block 63 to 8	3FFFFFFh-080000h	3584KB	Upper 56/64
1	1	0	1	Block 63 to 16	3FFFFFFh-100000h	3072KB	Upper 48/64
1	1	1	0	Block 63 to 32	3FFFFFFh-200000h	2048KB	Upper 32/64
1	1	1	1	All	000000h-3FFFFFFh	4096KB	All



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AT25DF321A :

WP State	Current SPRL Value	New Write Status Register Byte 1 Data	Protection Operation	New SPRL Value
		Bit 7 6 5 4 3 2 1 0		
0	0	0 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1	0
		0 x 0 0 0 1 x x		0
		↓		0
		0 x 1 1 1 0 x x		0
		0 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	0
		1 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1	1
		1 x 0 0 0 1 x x		1
		↓		1
1 x 1 1 1 0 x x	1			
1 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	1		
0	1	x x x x x x x x	No change to the current protection level. All sectors currently protected will remain protected and all sectors currently unprotected will remain unprotected. The Sector Protection Registers are hard-locked and cannot be changed when the WP pin is LOW and the current state of SPRL is 1. Therefore, a Global Protect/Unprotect will not occur. In addition, the SPRL bit cannot be changed (the WP pin must be HIGH in order to change SPRL back to a 0).	
1	0	0 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1	0
		0 x 0 0 0 1 x x		0
		↓		0
		0 x 1 1 1 0 x x		0
		0 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	0
		1 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1	1
		1 x 0 0 0 1 x x		1
		↓		1
1 x 1 1 1 0 x x	1			
1 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	1		
1	1	0 x 0 0 0 0 x x	No change to the current protection level. All sectors currently protected will remain protected, and all sectors currently unprotected will remain unprotected. The Sector Protection Registers are soft-locked and cannot be changed when the current state of SPRL is 1. Therefore, a Global Protect/Unprotect will not occur. However, the SPRL bit can be changed back to a 0 from a 1 since the WP pin is HIGH. To perform a Global Protect/Unprotect, the Write Status Register command must be issued again after the SPRL bit has been changed from a 1 to a 0.	0
		0 x 0 0 0 1 x x		0
		↓		0
		0 x 1 1 1 0 x x		0
		0 x 1 1 1 1 x x		0
		1 x 0 0 0 0 x x		1
		1 x 0 0 0 1 x x		1
		↓		1
1 x 1 1 1 0 x x	1			
1 x 1 1 1 1 x x		1		



4.2.2 Different Status Register bit definition

EN25Q32A :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

AT25DF321A :

Status Register Format – Byte 1

Bit ⁽¹⁾	Name		Type ⁽²⁾	Description	
7	SPRL	Sector Protection Registers Locked	R/W	0	Sector Protection Registers are unlocked (default).
				1	Sector Protection Registers are locked.
6	RES	Reserved for future use	R	0	Reserved for future use.
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	WPP	Write Protect (\overline{WP}) Pin Status	R	0	\overline{WP} is asserted.
				1	\overline{WP} is deasserted.
3:2	SWP	Software Protection Status	R	00	All sectors are software unprotected (all Sector Protection Registers are 0).
				01	Some sectors are software protected. Read individual Sector Protection Registers to determine which sectors are protected.
				10	Reserved for future use.
				11	All sectors are software protected (all Sector Protection Registers are 1 – default).
1	WEL	Write Enable Latch Status	R	0	Device is not write enabled (default).
				1	Device is write enabled.
0	RDY/BSY	Ready/Busy Status	R	0	Device is ready.
				1	Device is busy with an internal operation.

- Notes:
1. Only bit 7 of Status Register Byte 1 will be modified when using the Write Status Register Byte 1 command.
 2. R/W = Readable and writeable
R = Readable only



Status Register Format – Byte 2

Bit ⁽¹⁾	Name		Type ⁽²⁾	Description	
7	RES	Reserved for future use	R	0	Reserved for future use.
6	RES	Reserved for future use	R	0	Reserved for future use.
5	RES	Reserved for future use	R	0	Reserved for future use.
4	RSTE	Reset Enabled	R/W	0	Reset command is disabled (default).
				1	Reset command is enabled.
3	SLE	Sector Lockdown Enabled	R/W	0	Sector Lockdown and Freeze Sector Lockdown State commands are disabled (default).
				1	Sector Lockdown and Freeze Sector Lockdown State commands are enabled.
2	PS	Program Suspend Status	R	0	No sectors are program suspended (default).
				1	A sector is program suspended.
1	ES	Erase Suspend Status	R	0	No sectors are erase suspended (default).
				1	A sector is erase suspended.
0	RDY/BSY	Ready/Busy Status	R	0	Device is ready.
				1	Device is busy with an internal operation.

- Notes: 1. Only bits 4 and 3 of Status Register Byte 2 will be modified when using the Write Status Register Byte 2 command.
 2. R/W = Readable and writeable
 R = Readable only

Write Status Register Byte 1 Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPRL	X	Global Protect/Unprotect				X	X

Write Status Register Byte 2 Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	RSTE	SLE	X	X	X



4.2.3 Secured OTP Addresses

EN25Q32A:

Sector	Sector Size	Address Range
1023	512 byte	3FF000h – 3FF1FFh

Note: The OTP sector is mapping to sector 1023

AT25DF321A:

Security Register Byte Number									
0	1	...	62	63	64	65	...	126	127
One-Time User Programmable					Factory Programmed by Atmel				



4.2.4 The instructions comparison

Instructions	Command	EN25Q32A	AT25DF321A
EQIO (Full Quad Mode)	38h	Yes	No
RSTQIO (Reset Quad I/O)	FFh	Yes	No
Write Enable	06h	Yes	Yes
Write Disable / Exit OTP mode	04h	Yes	Yes (only for Write Disable)
Read Status Register	05h	Yes	Yes
Write Status Register	01h	Yes	Yes (Write Status Register Byte 1)
Write Status Register Byte 2	31h	No	Yes
Read Data	03h	Yes	Yes
Fast Read	0Bh	Yes	Yes
Read Array	1Bh	No	Yes
Dual Output Fast Read	3Bh	Yes	Yes
Dual I/O Fast Read	BBh	Yes	No
Quad I/O Fast Read	EBh	Yes	No
Page Program	02h	Yes	Yes
Dual Input Byte/Page Program	A2h	No	Yes
Sector Erase (4 KB) / OTP erase	20h	Yes	Yes (only for Sector Erase)
Block Erase (32 KB)	52h	No	Yes
Block Erase (64 KB)	D8h	Yes	Yes
Chip Erase	C7h / 60h	Yes	Yes
Program / Erase Suspend	B0h	No	Yes
Program / Erase Resume	D0h	No	Yes
Protect Sector	36h	No	Yes
Unprotect Sector	39h	No	Yes
Read Sector Protection Registers	3Ch	No	Yes
Sector Lockdown	33h	No	Yes
Freeze Sector Lockdown State	34h	No	Yes
Read Sector Lockdown Registers	35h	No	Yes
Program OTP Security Register	9Bh	No	Yes
Read OTP Security Register	77h	No	Yes
Reset	F0h	No	Yes
Deep Power-down	B9h	Yes	Yes
Release from Deep Power-down, and read Device ID	ABh	Yes	Yes
Release from Deep Power-down			
Manufacturer/ Device ID	90h	Yes	No
Read Identification	9Fh	Yes	Yes
Enter OTP mode	3Ah	Yes	No



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q32A		AT25DF321A		Unit
	Typ	Max	Typ	Max	
Page Programming Time	1.3	5	1.0	3	ms
Sector / Block Erase Time (4KB size)	0.09	0.3	0.05	0.2	sec
Block Erase Time (32KB size)	N/A	N/A	0.25	0.6	sec
Block Erase Time (64KB size)	0.5	2	0.4	0.95	sec
Chip (Bulk) Erase Time	25	50	32	56	sec

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q32A	AT25DF321A
tCH (serial clock high time)	Min @ 4ns	Min @ 4.3ns
tCL (serial clock low time)	Min @ 4ns	Min @ 4.3ns
tCLCH (serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCLCL (serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCHSH (CS# active setup / hold time)	Min @ 5ns	Min @ 5ns
tSHSL (CS# high time)	Min, read @ 15ns Program/Erase @ 50ns	Min @ 50ns
tDSU (Data in setup time)	Min @ 2ns	Min @ 2ns
tDH (Data in hold time)	Min @ 5ns	Min @ 1ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2010/02/25