



# **Application Note**

**EON EN25Q80A**

**VS**

**Numonyx M25PE80**

## **Specification Comparison**



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## 1. INTRODUCTION

The application note introduces how to implement a system design from Numonyx M25PE80 Flash to Eon EN25Q80A Flash.

## 2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q80A	M25PE80
Voltage Range	2.7 ~ 3.6	2.7 ~ 3.6
SPI frequency (standard / dual / quad mode)	100MHz (standard mode) 80MHz @ dual & quad mode	75MHz (standard mode)
Secured Silicon Sector Region	256 Byte	No
Sector Architecture	Uniform 256 Sectors of 4 K byte 16 Blocks of 64 K byte	Uniform Subsectors of 4 K byte Sectors of 64 K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
EQIO mode (Full Quad mode)	Yes	No
Dual Output Fast Read	Yes	No
Dual I/O Fast Read	Yes	No
Quad I/O Fast Read	Yes	No
Reset# pin	No	Yes
Page write	No	Yes
Page erase	No	Yes
Lock Register	No	Yes
Minimum Endurance Cycle	100K	100K
Package	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	SO8W (208mil) SO8N (150mil) VFQFPN8 5x6mm (MLP8) QFN8L 5x6mm (MLP8) / exposed pad of 3x3mm



## 3. HARDWARE CONSIDERATIONS

### 3.1 I<sub>CC</sub> comparison

Current	EN25Q80A	M25PE80	Unit
	Max	Max	
Read I <sub>CC3</sub>	25 @ 100MHz 20 @ 80MHz	8 @ 50MHz 6 @ 33MHz 12 @ 75MHz (for T9HX) 4 @ 33MHz (for T9HX)	mA
Page Program (PP) I <sub>CC4</sub>	28	15	mA
Sector Erase (SE) I <sub>CC6</sub> Block Erase (BE) I <sub>CC7</sub>	25	15	mA
Standby I <sub>CC1</sub>	5	50	μA

### 3.2 Pin Configuration

Pin number	EN25Q80A	M25PE80
Pin1	CS#	S#(CS#)
Pin2	DO (DQ1)	Q(DO)
Pin3	WP# (DQ2)	TSL# for T7Y process or W#(WP#) for T9HX process
Pin4	VSS	VSS
Pin5	DI (DQ0)	D(DI)
Pin6	CLK	C(CLK)
Pin7	NC (DQ3)	Reset#
Pin8	VCC	VCC

**Note:**

1. If customers don't use [Reset# pin](#) function on M25PE80, which can be replaced by EN25Q80A in [standard SPI mode](#).
2. M25PE80 only support general standard SPI mode.
3. EN25Q80A can support general standard / [dual](#) / [quad](#) SPI mode.  
(Need specific SPI controller)



## 4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

### For EN25Q80A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	3014h	

### For M25PE80

Manufacturer identification	Device identification		UID <sup>(1)</sup>	
	Memory type	Memory capacity	CFD length	CFD content
20h	80h	14h	10h	16 bytes

(1) The unique ID code is available only in the T9HX process



## 4.2. Instruction Set Comparison

### 4.2.1 Different Read Status Register content

**EN25Q80A :**

**S5 is reserved bit, S6 is WPDIS bit, S7 are SRP bit and OTP\_LOCK bit (in OTP mode).**

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

**M25PE80 :**

**Status register format<sup>(1) (2) (3)</sup>**

b7				b0			
SRWD	0	0	BP2	BP1	BP0	WEL	WIP

1. WEL (write enable latch) and WIP ((write in program) are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).
2. SRWD = status register write protect bit; BP0, BP1, BP2 = block protect bits.
3. The BP bits and the SRWD bit exist only in the T9HX process.



## 4.2.2 Different Lock Register content

EN25Q80A : No support.

M25PE80 :

### Lock registers

Bit	Bit name	Value	Function
b7-b4	Reserved		
b1	Sector lock down	'1'	The write lock and lock down bits cannot be changed. Once a '1' is written to the lock down bit it cannot be cleared to '0', except by a reset or power-up.
		'0'	The write lock and lock down bits can be changed by writing new values to them (default value).
b0	Sector write lock	'1'	Write, program and erase operations in this sector will not be executed. The memory contents will not be changed.
		'0'	Write, program and erase operations in this sector are executed and will modify the sector contents (default value).



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## Not for new design: lock registers for the M25PE80 in T7Y process

Bit	Bit name	Value	Function
b7-b4	Reserved		
b3	Subsector lock down <sup>(2)</sup>	'1'	This functionality must not be used for new designs, as the M25PE80 delivered from Feb 2007 will not offer this functionality. The write lock and lock down bits cannot be changed. Once a '1' is written to the lock down bit it cannot be cleared to '0' except by a reset or power-up.
		'0'	This functionality must not be used for new designs, as the M25PE80 delivered from Feb 2007 will not offer this functionality. The write lock and lock down bits can be changed by writing new values to them (default value).
b2	Subsector write lock <sup>(2)</sup>	'1'	This functionality must not be used for new designs, as the M25PE80 delivered from Feb 2007 will not offer this functionality. Write, program and erase operations in this subsector will not be executed. The memory contents will not be changed.
		'0'	This functionality must not be used for new designs, as the M25PE80 delivered from Feb 2007 will not offer this functionality. Write, program and erase operations in this subsector are executed and will modify the subsector contents (default value).
b1	Sector lock down	'1'	The write lock and lock down bits cannot be changed. Once a '1' is written to the lock down bit it cannot be cleared to '0', except by a reset or power-up.
		'0'	The write lock and lock down bits can be changed by writing new values to them (default value).
b0	Sector write lock	'1'	Write, program and erase operations in this sector will not be executed. The memory contents will not be changed.
		'0'	Write, program and erase operations in this sector are executed and will modify the sector contents (default value).

1. Valid only for sector 0 and sector 15 (the value '0' is returned for other sectors).



## 4.2.3 Different software protections

### EN25Q80A : Block protect area definitions of (BP0~BP2)

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 253	000000h-0FDFFFh	1016KB	Lower 254/256
0	1	0	Sector 0 to 251	000000h-0FBFFFh	1008KB	Lower 252/256
0	1	1	Sector 0 to 247	000000h-0F7FFFh	992KB	Lower 248/256
1	0	0	Sector 0 to 239	000000h-0EFFFFh	960KB	Lower 240/256
1	0	1	Sector 0 to 223	000000h-0DFFFFh	896KB	Lower 224/256
1	1	0	Sector 0 to 191	000000h-0BFFFFh	768KB	Lower 192/256
1	1	1	All	000000h-0FFFFFFh	1024KB	All

### M25PE80 :

#### The first software protected mode (SPM1)

#### Software protection truth table (sectors 0 to 15, 64-Kbyte granularity)

Sector lock register		Protection status
Lock down bit	Write lock bit	
0	0	Sector unprotected from program/erase/write operations, protection status reversible
0	1	Sector protected from program/erase/write operations, protection status reversible
1	0	Sector unprotected from program/erase/write operations, Sector protection status cannot be changed except by a reset or power-up.
1	1	Sector protected from program/erase/write operations, Sector protection status cannot be changed except by a reset or power-up.



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Not for new design: TY7 process only, software protection scheme truth table (sectors 0 and 15)

Sector lock register		Subsector lock register		Protection status
Lock down bit	Write lock bit	Lock down bit	Write lock bit	
0	0	0	0	Current subsector unprotected from program/erase/write operations, Current subsector protection status reversible
		0	1	Current subsector protected from program/erase/write operations, Current subsector protection status reversible.
		1	0	Current subsector unprotected from program/erase/write operations, current subsector protection status cannot be changed except by a reset or power-up.
		1	1	Current subsector protected from program/erase/write operations, Current subsector protection status cannot be changed except by a reset or power-up.
	1	0	1	All subsectors protected from program/erase/write operations, current subsector protection status reversible
		1	1	All subsectors protected from program/erase/write operations, current subsector protection status cannot be changed except by a reset or power-up.
1	0	1	0	Current subsector unprotected from program/erase/write operations, all subsectors protection status cannot be changed except by a reset or power-up
		1	1	Current subsector protected from program/erase/write operations, all subsectors protection status cannot be changed except by a reset or power-up
	1	1	1	All subsectors protected with their protection status cannot be changed except by a reset or power-up.



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## M25PE80 :

The second software protected mode (SPM2) uses the block protect (BP2, BP1, BP0)

### Protected area sizes

Status register content			Memory content	
BP2 bit	BP1 bit	BP0 bit	Protected area	Unprotected area
0	0	0	none	All sectors <sup>(1)</sup> (sixteen sectors: 0 to 15)
0	0	1	Upper sixteenth (Sector 15)	Lower fifteen-sixteenths (fifteen sectors: 0 to 14)
0	1	0	Upper eighth (two sectors: 14 and 15)	Lower seven-eighths (fourteen sectors: 0 to 13)
0	1	1	Upper quarter (four sectors: 12 to 15)	Lower three-quarters (twelve sectors: 0 to 11)
1	0	0	Upper half (eight sectors: 8 to 15)	Lower half (eight sectors: 0 to 7)
1	0	1	All sectors (sixteen sectors: 0 to 15)	none
1	1	0	All sectors (sixteen sectors: 0 to 15)	none
1	1	1	All sectors (sixteen sectors: 0 to 15)	none

1. The device is ready to accept a bulk erase instruction if, and only if, all block protect (BP2, BP1, BP0) are 0.

#### 4.2.4 Enable Quad I/O (EQIO) (38h) command

EN25Q80A : Support.

M25PE80 : No support.

#### 4.2.5 Reset Quad I/O (RSTQIO) (FFh) command

EN25Q80A : Support.

M25PE80 : No support.

#### 4.2.6 Dual Output Fast Read (3Bh) commands

EN25Q80A : Support.

M25PE80 : No support.

#### 4.2.7 Dual Input / Output FAST\_READ (BBh) commands

EN25Q80A : Support.

M25PE80 : No support.



## 4.2.8 Quad Input / Output FAST\_READ (EBh) commands

EN25Q80A : Support.

M25PE80 : No support.

## 4.2.9 Manufacturer/ Device ID (90h) commands

EN25Q80A : Support.

M25PE80 : No support.

## 4.2.10 Enter OTP Mode (3Ah) commands

EN25Q80A : Support.

### OTP Sector Address

Sector	Sector Size	Address Range
255	256 byte	0FF000h – 0FF0FFh

Note: The OTP sector is mapping to sector 255

M25PE80 : No support.

## 4.2.11 Write to lock register (E5h) commands

EN25Q80A : No support.

M25PE80 : Support.

## 4.2.12 Read lock register (E8h) commands

EN25Q80A : No support.

M25PE80 : Support.

## 4.2.13 Page write (0Ah) commands

EN25Q80A : No support.

M25PE80 : Support.

## 4.2.14 Page erase (DBh) commands

EN25Q80A : No support.

M25PE80 : Support.



## 5. PERFORMANCE DIFFERENCES

### 5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q80A		M25PE80 (75MHz, T9XH)		Unit
	Typ	Max	Typ	Max	
Page Programming Time	1.3	5	0.8	3	ms
4 KB Sector Erase Time	0.09	0.3	0.05	0.15	sec
64KB Block Erase Time	0.5	2	1	5	sec
Chip (Bulk) Erase Time	8	20	10	60	sec

### 5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q80A	M25PE80 (75MHz, T9XH)
tCH (serial clock high time)	Min @ 4ns	Min @ 6ns
tCL (serial clock low time)	Min @ 4ns	Min @ 6ns
tCLCH(serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCLCL(serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
tSHSL(CS# high time)	Min @ 15ns for Read Min @ 50ns for Write	Min @ 100ns
tDSU(Data in setup time)	Min @ 2ns	Min @ 2ns
tDH(Data in hold time)	Min @ 5ns	Min @ 5ns



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## Revisions List

Revision No	Description	Date
A	Initial Release	2010/05/11