Migration Note

Eon Flash

	P/N	Datasheet Version
From	EN29LV640T/B	Rev. H
To	EN29LV640AT/B	Rev. B

1. INTRODUCTION

The migration note introduces how to implement a system design from Eon flash EN29LV640T/B to EN29LV640AT/B.

2. GENERAL FUNCTION COMPARISON TABLE:

The following table is major features of these two devices.

Features	EN29LV640T/B	EN29LV640AT/B
Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Pin to Pin	48-pin TSOP (Type 1) 48-ball 6mm x 8mm TFBGA	48-pin TSOP (Type 1) 48-ball 6mm x 8mm TFBGA
Access Time	- Full voltage range (2.7V~3.6V): Access times as fast as 90 ns - Regulated voltage range (3.0V~3.6V): Access times as fast as 70ns	90ns
Sector Architecture	8K-byte x8 32K-Word/64K-byte x127	8K-byte x8 32K-Word/64K-byte x127
Secured Silicon Sector	N/A	128-Word/256-byte x1
Byte/Word Mode	Yes	Yes
V_{ID} and V_{HH} Range	10.5V – 11.5V	8.5V – 9.5V
Erase Suspend/Resume	Yes	Yes
Minimum Endurance Cycle	100K	100K
Package	48-pin TSOP (Type 1) 48-ball 6mm x 8mm TFBGA	48-pin TSOP (Type 1) 48-ball 6mm x 8mm TFBGA

3. HARDWARE CONSIDERATIONS

3.1. I_{CC} Comparison

Current	EN29LV640T/B		EN29LV640AT/B		Unit
	Typ	Max	Typ	Max	
Read I_{CC1}	9	16	9	16	mA
Write I_{CC2}	20	30	20	30	mA
Standby I_{CC3}	1	5.0	1	5.0	μA

Note：There is no difference between EN29LV640T/B and EN29LV640AT/B.

3.2. Pin Descriptions

EN29LV640T/B		EN29LV640AT/B	
Pin Name	**Function**	**Pin Name**	**Function**
A0-A21	22 Address inputs	A0-A21	22 Address inputs
DQ0-DQ14	15 Data Inputs/Outputs	DQ0-DQ14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)	DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable	CE#	Chip Enable
OE#	Output Enable	OE#	Output Enable
WE#	Write Enable	WE#	Write Enable
WP# / ACC	Write Protect / Acceleration Pin	WP# / ACC	Write Protect / Acceleration Pin
RESET#	Hardware Reset Pin	RESET#	Hardware Reset Pin
BYTE#	Byte/Word Mode Selection	BYTE#	Byte/Word Mode Selection
RY/BY#	Ready/Busy Output	RY/BY#	Ready/Busy Output
Vcc	Supply Voltage (2.7-3.6V)	Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground	Vss	Ground
NC	Not Connected to anything	NC	Not Connected to anything

Note：There is no difference between EN29LV640T/B and EN29LV640AT/B.

4. Autoselect Codes (Using High Voltage, V_{ID})

64M FLASH MANUFACTURER/DEVICE ID TABLE

Description		CE#	OE#	WE#	A21 to A12	A11 to A10	A9[2]	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Eon		L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	L	X	1Ch
								L							7Fh
Device ID (top boot sector)	Word	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	22h	C9h
	Byte	L	L	H										X	C9h
Device ID (bottom boot sector)	Word	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	22h	CBh
	Byte	L	L	H										X	CBh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	X	L	X	H	L	X	01h (Protected)
														X	00h (Unprotected)

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} = 9 ± 0.5V, X=Don't Care (either L or H, but not floating!), SA=Sector Addresses

Note:

1. A8 = H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.
3. There is no difference between EN29LV640T/B and EN29LV640AT/B.

5. SOFTWARE CONSIDERATIONS

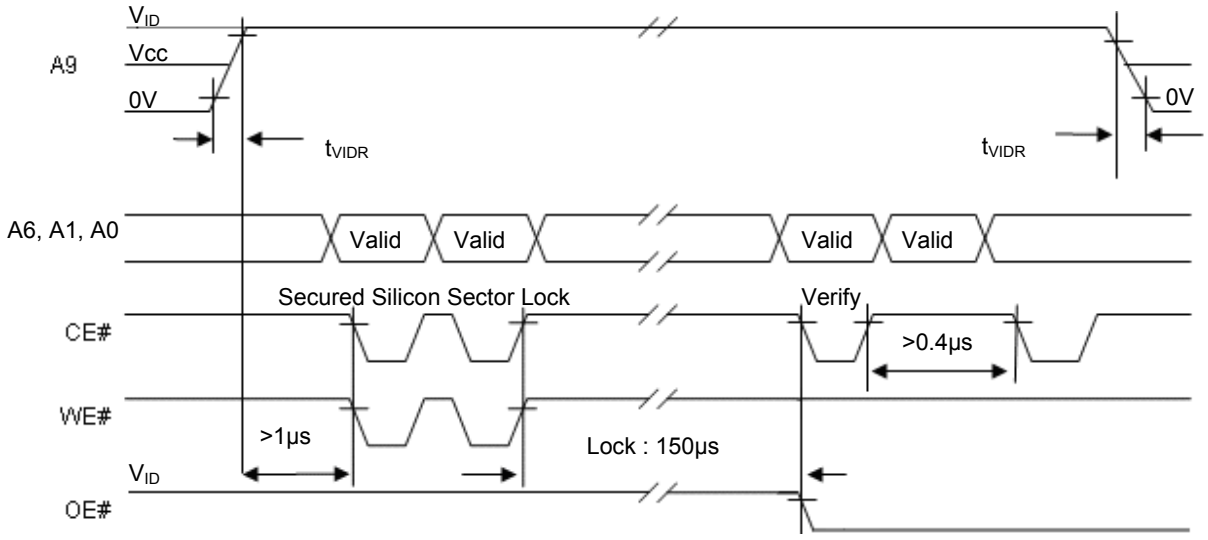
5.1. 64M FLASH SECURED SILICON SECTOR TABLE[1]

Description	CE#	OE#	WE#	A21 to A12	A11 to A10	A9[2]	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Secured Silicon Sector Lock[3]	L	V_{ID}	⎍	X	X	V_{ID}	X	X	L	X	H	L	X	X
Secured Silicon Sector Lock Bit Verification (DQ0)[3]	L	L	H	X	X	V_{ID}	X	X	L	X	H	L	X	X1h (Locked) X0h (Unlocked)

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} = 9 ± 0.5V, X=Don't Care (either L or H, but not floating!), SA=Sector Addresses

Note:

1. 64M FLASH SECURED SILICON SECTOR TABLE is valid only in Secured Silicon Sector which exists at EN29LV640AT/B.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.
3. AC Waveform for Secured Silicon Sector Lock / Verification Operations Timings.



5.1.1. Top Boot Security Sector Address Table

Sector Address A21 ~ A12	Sector Size (bytes / words)	Address Range (h) Byte Mode (x8)	Address Range (h) Word Mode (x16)
1111111111	256 / 128	7FFF00–7FFFFF	3FFF80–3FFFFF

5.1.2. Bottom Boot Security Sector Address Table

Sector Address A21 ~ A12	Sector Size (bytes / words)	Address Range (h) Byte Mode (x8)	Address Range (h) Word Mode (x16)
0000000000	256 / 128	000000–0000FF	000000–00007F

5.2. Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1P[stP] Cycle		2P[ndP] Cycle		3P[rdP] Cycle		4P[thP] Cycle		5P[thP] Cycle		6P[thP] Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
										100	1C				
		Byte		AAA		555		AAA		000	7F				
										200	1C				
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	x01	22C9				
		Byte		AAA		555		AAA		x02	C9				
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	x01	22CB				
		Byte		AAA		555		AAA		x02	CB				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA) X02	00				
											01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
											08*				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Sector Erase Suspend			1	XXX	B0										
Sector Erase Resume			1	XXX	30										
CFI Query		Word	1	55	98										
		Byte		AA											
Enter Secured Silicon Sector*		Word	3	555	AA	2AA	55	555	88						
		Byte		AAA		555		AAA							
Exit Secured Silicon Sector*		Word	4	555	AA	2AA	55	555	90	xxx	00				
		Byte		AAA		555		AAA		xxx	00				

Address and Data values indicated are in hex. Unless specified, all bus cycles are write cycles

RA = Read Address: address of the memory location to be read. This is a read cycle.

RD = Read Data: data read from location RA during Read operation. This is a read cycle.

PA = Program Address: address of the memory location to be programmed. X = Don't-Care

PD = Program Data: data to be programmed at location PA

SA = Sector Address: address of the Sector to be erased or verified. Address bits A20-A12 uniquely select any Sector.

Note：

* Only available at EN29LV640AT/B.

6. PERFORMANCE DIFFERENCES

6.1. Power-On and Hardware Reset (RESET#) Timings

Parameter	Description	EN29LV640T/B	EN29LV640AT/B
t_{VCS}	Vcc Setup Time	50µs	50µs
t_{RP1}	RESET# Pulse Width (During Embedded Algorithms)	10us	10µs
t_{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	500ns	500ns
t_{RH}	Reset# High Time Before Read	50ns	50ns
t_{RB1}	RY/BY# Recovery Time (to CE#, OE# go low)	0ns	0ns
t_{RB2}	RY/BY# Recovery Time (to WE# go low)	50ns	50ns
t_{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	20µs	20µs
t_{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	500ns	500ns

6.2. ERASE AND PROGRAM PERFORMANCE

The ERASE and PROGRAM Performance Comparison

Parameter		EN29LV640T/B		EN29LV640AT/B		Unit
		Typ	Max	Typ	Max	
Sector Erase Time		0.1	2	0.1	2	sec
Chip Erase Time		16	140	16	140	sec
Byte Programming Time		8	200	8	200	µs
Word Programming Time		8	200	8	200	µs
Accelerated Byte/Word Program Time		7	120	7	200	µs
Chip Programming Time	Byte	67.2	201.6	67.2	201.6	sec
	Word	33.6	100.8	33.6	100.8	sec
Word Programming Time		100K		100K		Cycles

Notes:

1. Typical program and erase times assume the following conditions: room temperature, 3V and checkerboard pattern programmed.
2. Maximum program and erase times assume the following conditions: worst case Vcc, 90°C and 100,000 cycles.

Revisions List

Revision No	Description	Date
A	Initial Release	2010/08/09