



Application Note

EON EN25Q32A

(Version : d)

VS

MXIC MX25L3235D

(Version : 1.4)



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1. INTRODUCTION

The application note introduces how to implement a system design from MXIC MX25L3235D Flash to Eon EN25Q32A Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q32A	MX25L3235D
Voltage range	2.7 ~ 3.6V	2.7 ~ 3.6V
Pin to pin compatible (standard SPI mode)	8 pins SOP 200mil 8 contact VDFN (5 x 6mm) 16 pins SOP 300mil	8-pin SOP 209mil 8-land WSON (6 x 5mm) 16-pin SOP 300mi
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI frequency (standard mode)	100MHz (standard mode) 80MHz @ dual & quad mode	104MHz (standard mode) 75MHz @ dual & quad mode
Sector architecture	Uniform 1024 sectors of 4K byte 64 blocks of 64K byte	Uniform 1024 sectors of 4K byte 64 blocks of 64K byte
Lockable OTP security sector	512 Byte	512 Byte
Minimum endurance cycle	100K	100K
Package	8 pins SOP 200mil 8 contact VDFN (5 x 6mm) 8 pins PDIP 16 pins SOP 300mil	8-pin SOP 209mil 8-land WSON (6 x 5mm, 8 x 6mm) 16-pin SOP 300mil



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q32A	MX25L3235D	Unit
	Max (@ Single 100MHz)	Max (@Single 104MHz)	
Read I _{CC3}	25	25	mA
Page Program (PP) I _{CC4}	28	20	mA
Sector Erase (SE) I _{CC6}	25	20	mA
Standby I _{CC1}	20	20	μA



4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

For EN25Q32A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			15h
90h	1Ch		15h
9Fh	1Ch	3016h	

For MX25L3235D

Command Type	MX25L3235D		
RDID Command (JEDEC)	manufacturer ID	memory type	memory density
	C2	5E	16
RES Command	electronic ID		
	5E		
REMS/REMS2/REMS4/ Command	manufacturer ID	device ID	
	C2	5E	



4.2. Instruction set comparison

EN25Q32A

MX25L3235D does not support [Dual Output Fast Read](#) instruction, and The [Enter OTP mode instruction](#) for EN25Q32A is 3Ah while the instruction for MX25L3235D is B1h.

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQIO	38h						
RSTQIO(1)	FFh						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0)(2)					continuous(3)
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(4)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(5)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(6)		
Enter OTP mode	3Ah						

Notes:

1. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode.
2. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis () indicate data being read from the device on the DO pin.
3. The Status Register contents will repeat continuously until CS# terminate the instruction.
4. The Device ID will repeat continuously until CS# terminates the instruction.
5. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction.
00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
6. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.



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Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) ⁽¹⁾	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8 ⁽²⁾	A7-A0, dummy ⁽²⁾	(D7-D0, ...) ⁽¹⁾			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh	A23-A0, dummy ⁽⁴⁾	(dummy, D7-D0) ⁽⁵⁾	(D7-D0, ...) ⁽³⁾			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data

DQ₀ = (D6, D4, D2, D0)

DQ₁ = (D7, D5, D3, D1)

2. Dual Input Address

DQ₀ = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, dummy 6, dummy 4, dummy 2, dummy 0

DQ₁ = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, dummy 7, dummy 5, dummy 3, dummy 1

3. Quad Data

DQ₀ = (D4, D0,)

DQ₁ = (D5, D1,)

DQ₂ = (D6, D2,)

DQ₃ = (D7, D3,)

4. Quad Input Address

DQ₀ = A20, A16, A12, A8, A4, A0, dummy 4, dummy 0

DQ₁ = A21, A17, A13, A9, A5, A1, dummy 5, dummy 1

DQ₂ = A22, A18, A14, A10, A6, A2, dummy 6, dummy 2

DQ₃ = A23, A19, A15, A11, A7, A3, dummy 7, dummy 3

5. Quad I/O Fast Read Data

DQ₀ = (dummy 12, dummy 8, dummy 4, dummy 0, D4, D0)

DQ₁ = (dummy 13, dummy 9, dummy 5, dummy 1, D5, D1)

DQ₂ = (dummy 14, dummy 10, dummy 6, dummy 2, D6, D2)

DQ₃ = (dummy 15, dummy 11, dummy 7, dummy 3, D7, D3)



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MX25L3235D

EN25Q32A does not support [Continuously program mode](#), [REMS2](#), [REMS4](#), [EXSO RDSCUR](#), [WRSCUR](#), [ESRY](#), [DSRY](#) instructions.

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)	2READ (2 x I/O read command) Note 1
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	03 (hex)	0B (hex)	BB (hex)
2nd byte						AD1 (A23-A16)	AD1	ADD(2)
3rd byte						AD2 (A15-A8)	AD2	ADD(2) & Dummy(2)
4th byte						AD3 (A7-A0)	AD3	
5th byte							Dummy	
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high
								↓
COMMAND (byte)	4READ (4 x I/O read command)	Release Read Enhanced	4PP (quad page program)	SE (sector erase)	BE (block erase)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)
1st byte	EB (hex)	FFh (hex)	38 (hex)	20 (hex)	D8 (hex)	60 or C7 (hex)	02 (hex)	AD (hex)
2nd byte	ADD(4) & Dummy(4)	x	AD1	AD1	AD1		AD1	AD1
3rd byte	Dummy(4)	x		AD2	AD2		AD2	AD2
4th byte		x		AD3	AD3		AD3	AD3
5th byte								
Action	n bytes read out by 4 x I/O until CS# goes high	All these commands FFh,00h,AAh or 55h will escape the performance enhance mode	quad input to program the selected page	to erase the selected sector	to erase the selected block	to erase whole chip	to program the selected page	continuously program whole chip, the address automatically increases
				↓	↓	↓	↓	↓
COMMAND (byte)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)
1st byte	B9 (hex)	AB (hex)	AB (hex)	90 (hex)	EF (hex)	DF (hex)	B1 (hex)	C1 (hex)
2nd byte			x	x	x	x		
3rd byte			x	x	x	x		
4th byte			x	ADD (Note 2)	ADD (Note 2)	ADD (Note 2)		
5th byte								
Action	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & device ID	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode



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COMMAND (byte)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/ BY#)	DSRY (disable SO to output RY/ BY#)
1st byte	2B (hex)	2F (hex)	70 (hex)	80 (hex)
2nd byte				
3rd byte				
4th byte				
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/ BY# during CP mode	to disable SO to output RY/ BY# during CP mode

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. The MSB is on SI/SIO1 which is different from 1 x I/O condition.

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 3: It is not allowed to adopt any other code which is not in the command definition table above, which will lead to entering the hidden mode.



4.3 Different block protection area

The definition of block protection area is different.

EN25Q32A

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 62	000000h-3EFFFFh	4032KB	Lower 63/64
0	0	1	0	Block 0 to 61	000000h-3DFFFFh	3968KB	Lower 62/64
0	0	1	1	Block 0 to 59	000000h-3BFFFFh	3840KB	Lower 60/64
0	1	0	0	Block 0 to 55	000000h-37FFFFh	3584KB	Lower 56/64
0	1	0	1	Block 0 to 47	000000h-2FFFFFFh	3072KB	Lower 48/64
0	1	1	0	Block 0 to 31	000000h-1FFFFFFh	2048KB	Lower 32/64
0	1	1	1	All	000000h-3FFFFFFh	4096KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 63 to 1	3FFFFFFh-010000h	4032KB	Upper 63/64
1	0	1	0	Block 63 to 2	3FFFFFFh-020000h	3968KB	Upper 62/64
1	0	1	1	Block 63 to 4	3FFFFFFh-040000h	3840KB	Upper 60/64
1	1	0	0	Block 63 to 8	3FFFFFFh-080000h	3584KB	Upper 56/64
1	1	0	1	Block 63 to 16	3FFFFFFh-100000h	3072KB	Upper 48/64
1	1	1	0	Block 63 to 32	3FFFFFFh-200000h	2048KB	Upper 32/64
1	1	1	1	All	000000h-3FFFFFFh	4096KB	All

MX25L3235D

Status bit				Protect Level
BP3	BP2	BP1	BP0	32Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 63th)
0	0	1	0	2 (2blocks, block 62th-63th)
0	0	1	1	3 (4blocks, block 60th-63th)
0	1	0	0	4 (8blocks, block 56th-63th)
0	1	0	1	5 (16blocks, block 48th-63th)
0	1	1	0	6 (32blocks, block 32th-63th)
0	1	1	1	7 (64blocks, all)
1	0	0	0	8 (64blocks, all)
1	0	0	1	9 (32blocks, block 0th-31th)
1	0	1	0	10 (48blocks, block 0th-47th)
1	0	1	1	11 (56blocks, block 0th-55th)
1	1	0	0	12 (60blocks, block 0th-59th)
1	1	0	1	13 (62blocks, block 0th-61th)
1	1	1	0	14 (63blocks, block 0th-62th)
1	1	1	1	15 (64blocks, all)



4.4 Different RDSR bit definition

The definition of RDSR bit S6 and bit6 are different.

EN25Q32A



S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

MX25L325D



bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad enable 0=not Quad enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q32A		MX25L3235D		Unit
	Typ	Max	Typ	Max	
Page programming time	1.3	5	1.4	5	ms
Sector erase time	0.09	0.3	0.06	0.3	sec
Block erase time	0.5	2	0.7	2	sec
Chip (Bulk) erase time	25	50	25	50	sec

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q32A	MX25L3235D
t _{CH} (serial clock high time)	Min @ 4ns	Min @ 4.7ns
t _{CL} (serial clock low time)	Min @ 4ns	Min @ 4.7ns
t _{CLCH} (serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t _{CLCL} (serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t _{CHSH} (CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
t _{SHSL} (CS# high time)	Min @ 50ns	Min @ 5ns
t _{DSU} (Data in setup time)	Min @ 2ns	Min @ 2ns
t _{DH} (Data in hold time)	Min @ 5ns	Min @ 5ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2010/07/05