



Application Note

EON EN25Q32B

(Version : Preliminary 0.2)

VS

Winbond W25Q32BV

(Version : D)



1. INTRODUCTION

The application note introduces how to implement a system design from Winbond W25Q32BV Flash to Eon EN25Q32B Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q32B	W25Q32BV
Voltage range	2.7 ~ 3.6V	2.7 ~ 3.6V
Pin to pin compatible (standard SPI mode)	N/A	N/A
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI frequency (standard mode)	104MHz (standard mode) 80MHz @ dual & quad mode	104MHz (standard mode) 80MHz @ dual & quad mode
Sector architecture	Uniform 1024 sectors of 4K byte 64 blocks of 64K byte	Uniform 1024 sectors of 4K byte 128 blocks of 32K byte 64 blocks of 64K byte
Lockable OTP security sector	512 Byte	1K Byte
EQIO mode (Full quad mode)	Yes	No
Block erase 32K Byte	No	Yes
Program and erase suspend / resume	No	Yes
Minimum endurance cycle	100K	100K
Package	8 pins SOP 200mil 8 contact VDFN (5 x 6mm) 16 pins SOP 300mil 24 balls BGA (6 x 8mm)	8-pin SOIC 208mil 8-pad WSON (6 x 5mm, 8 x 6mm) 16-pin SOIC 300mil 8-pin PDIP 300mil



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

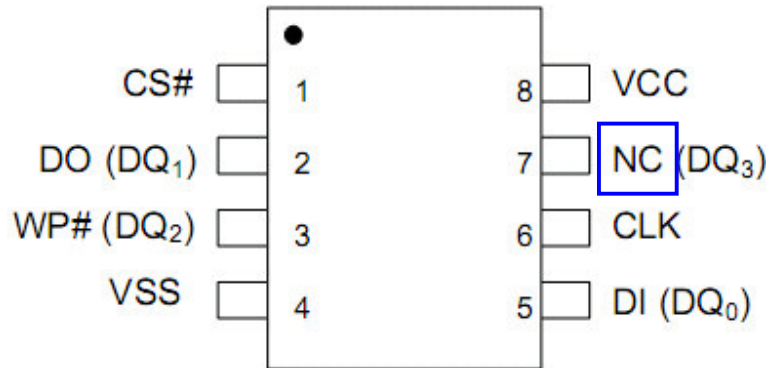
Current	EN25Q32B	W25Q32BV	Unit
	Max (@ Single 104MHz)	Max (@ Quad 80MHz)	
Read I _{CC3}	25	18	mA
Page Program (PP) I _{CC4}	28	25	mA
Sector Erase (SE) I _{CC6}	25	25	mA
Standby I _{CC1}	20	50	μA



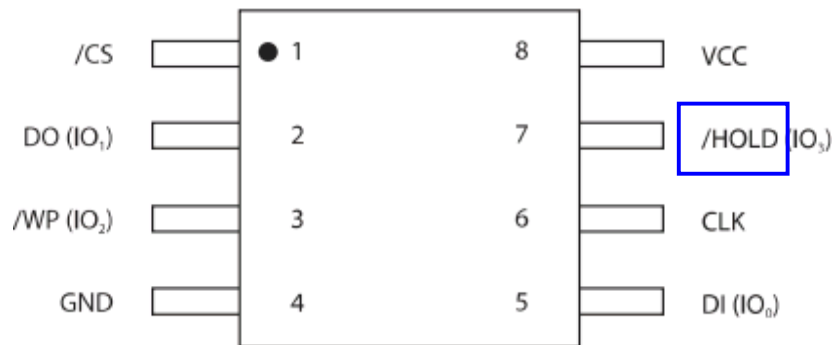
3.2 Pin Configuration

8-pin SOP 150mil

For EN25Q32B



For W25Q32BV





4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

For EN25Q32B

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			15h
90h	1Ch		15h
9Fh	1Ch	3016h	

For W25Q32BV

MANUFACTURER ID	(MF7-MF0)	
Winbond Serial Flash	EFh	
Device ID	(ID7-ID0)	(ID15-ID0)
Instruction	ABh, 90h	9Fh
W25Q32BV	15h	4016h



4.2. Instruction set comparison

EN25Q32B

W25Q32BV does not support [EQIO](#), [RSTQIO](#), [RSTEN](#), [RST](#), [Enter OTP mode](#) instructions.

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
→ EQIO	38h						
→ RSTQIO ⁽²⁾ / Release Quad I/O or Fast Read Enhanced Mode	FFh						
→ RSTEN	66h						
→ RST ⁽¹⁾	99h						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0) ⁽³⁾					continuous ⁽⁴⁾
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP Erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(5)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(6)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		
→ Enter OTP mode	3Ah						

Notes:

1. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
2. Device accepts eight-clcks command in Standard SPI mode, or two-clcks command in Quad SPI mode
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "(")" indicate data being read from the device on the DO pin
4. The Status Register contents will repeat continuously until CS# terminate the instruction
5. The Device ID will repeat continuously until CS# terminates the instruction
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction.
00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID
7. (M7-M0): Manufacturer, (ID15-ID8): Memory Type, (ID7-ID0): Memory Capacity



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W25Q32BV

EN25Q32B does not support Write Enable for Volatile Status Register, Read Status Register-2, Quad Page Program, Block Erase(32KB), Erase / Program Suspend, Erase / Program Resume, Continuous Read Mode Reset, Fast Read Quad Output, Word Read Quad I/O, Octal Word Read Quad I/O, Set Burst with Wrap, Read Manufacturer / Device ID by Dual I/O, Read Manufacturer / Device ID by Quad I/O, Read Unique ID, Erase Security Registers, Program Security Registers, Read Security Registers instructions.

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	06h					
Write Enable for Volatile Status Register	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0) ⁽²⁾				
Read Status Register-2	35h	(S15-S8) ⁽²⁾				
Write Status Register	01h	(S7-S0)	(S15-S8)			
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0, ...) ⁽³⁾	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h/60h					
Erase / Program Suspend	75h					
Erase / Program Resume	7Ah					
Power-down	B9h					
Continuous Read Mode Reset ⁽⁴⁾	FFh	FFh				

Notes:

- Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “()” indicate data being read from the device on the DO pin.
- The Status Register contents will repeat continuously until /CS terminates the instruction.
- Quad Page Program Input Data:
 - IO0 = (D4, D0,)
 - IO1 = (D5, D1,)
 - IO2 = (D6, D2,)
 - IO3 = (D7, D3,)
- This instruction is recommended when using the Dual or Quad “Continuous Read Mode” feature. See section 11.2.19 & 11.2.20 for more information.



INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) ⁽¹⁾
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) ⁽³⁾
Fast Read Dual I/O	BBh	A23-A8 ⁽²⁾	A7-A0, M7-M0 ⁽²⁾	(D7-D0, ...) ⁽¹⁾		
Fast Read Quad I/O	EBh	A23-A0, M7-M0 ⁽⁴⁾	(x,x,x,x, D7-D0, ...) ⁽⁵⁾	(D7-D0, ...) ⁽³⁾		
Word Read Quad I/O ⁽⁷⁾	E7h	A23-A0, M7-M0 ⁽⁴⁾	(x,x, D7-D0, ...) ⁽⁶⁾	(D7-D0, ...) ⁽³⁾		
Octal Word Read Quad I/O ⁽⁸⁾	E3h	A23-A0, M7-M0 ⁽⁴⁾	(D7-D0, ...) ⁽³⁾			
Set Burst with Wrap	77h	xxxxxx, W6-W4 ⁽⁴⁾				

Notes:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0,)

IO1 = (D5, D1,)

IO2 = (D6, D2,)

IO3 = (D7, D3,)

4. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap Input

IO0 = x, x, x, x, x, x, W4, x

IO1 = x, x, x, x, x, x, W5, x

IO2 = x, x, x, x, x, x, W6, x

IO3 = x, x, x, x, x, x, x

5. Fast Read Quad I/O Data

IO0 = (x, x, x, x, D4, D0,)

IO1 = (x, x, x, x, D5, D1,)

IO2 = (x, x, x, x, D6, D2,)

IO3 = (x, x, x, x, D7, D3,)

6. Word Read Quad I/O Data

IO0 = (x, x, D4, D0,)

IO1 = (x, x, D5, D1,)

IO2 = (x, x, D6, D2,)

IO3 = (x, x, D7, D3,)

7. The lowest address bit must be 0. (A0 = 0)

8. The lowest 4 address bits must be 0. (A0, A1, A2, A3 = 0)



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INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Release Power down / Device ID	ABh	dummy	dummy	dummy	(ID7-ID0) ⁽¹⁾	
Manufacturer/ Device ID ⁽²⁾	90h	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
→ Manufacturer/Device ID by Dual I/O	92h	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])		
→ Manufacture/Device ID by Quad I/O	94h	A23-A0, M[7:0]	xxxx, (MF[7:0], ID[7:0])	(MF[7:0], ID[7:0], ...)		
JEDEC ID	9Fh	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
→ Read Unique ID	4Bh	dummy	dummy	dummy	dummy	(ID63-ID0)
→ Erase Security Registers ⁽³⁾	44h	A23-A16	A15-A8	A7-A0		
→ Program Security Registers ⁽³⁾	42h	A23-A16	A15-A8	A7-A0	(D7-0)	(D7-0)
→ Read Security Registers ⁽³⁾	48h	A23-A16	A15-A8	A7-A0	dummy	(D7-0)

Notes:

1. The Device ID will repeat continuously until /CS terminates the instruction.
2. See Manufacturer and Device Identification table for Device ID information.
3. Security Register Address:

Security Register 0: A23-16 = 00h; A15-8 = 00h; A7-0 = byte address
 Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
 Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
 Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

Please note that Security Register 0 is reserved by Winbond for future use. It is recommended to use Security registers 1- 3 before using register 0.



4.3 Different block protection area

The definition of block protection area is different.

EN25Q32B

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 62	000000h-3EFFFFh	4032KB	Lower 63/64
0	0	1	0	Block 0 to 61	000000h-3DFFFFh	3968KB	Lower 62/64
0	0	1	1	Block 0 to 59	000000h-3BFFFFh	3840KB	Lower 60/64
0	1	0	0	Block 0 to 55	000000h-37FFFFh	3584KB	Lower 56/64
0	1	0	1	Block 0 to 47	000000h-2FFFFFFh	3072KB	Lower 48/64
0	1	1	0	Block 0 to 31	000000h-1FFFFFFh	2048KB	Lower 32/64
0	1	1	1	All	000000h-3FFFFFFh	4096KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 63 to 1	3FFFFFFh-010000h	4032KB	Upper 63/64
1	0	1	0	Block 63 to 2	3FFFFFFh-020000h	3968KB	Upper 62/64
1	0	1	1	Block 63 to 4	3FFFFFFh-040000h	3840KB	Upper 60/64
1	1	0	0	Block 63 to 8	3FFFFFFh-080000h	3584KB	Upper 56/64
1	1	0	1	Block 63 to 16	3FFFFFFh-100000h	3072KB	Upper 48/64
1	1	1	0	Block 63 to 32	3FFFFFFh-200000h	2048KB	Upper 32/64
1	1	1	1	All	000000h-3FFFFFFh	4096KB	All



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CMP = 0

STATUS REGISTER ⁽¹⁾					W25Q32BV (32M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION ⁽²⁾
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000h – 3FFFFFFh	64KB	Upper 1/64
0	0	0	1	0	62 and 63	3E0000h – 3FFFFFFh	128KB	Upper 1/32
0	0	0	1	1	60 thru 63	3C0000h – 3FFFFFFh	256KB	Upper 1/16
0	0	1	0	0	56 thru 63	380000h – 3FFFFFFh	512KB	Upper 1/8
0	0	1	0	1	48 thru 63	300000h – 3FFFFFFh	1MB	Upper 1/4
0	0	1	1	0	32 thru 63	200000h – 3FFFFFFh	2MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/64
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/32
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/16
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/8
0	1	1	0	1	0 thru 15	000000h – 0FFFFFFh	1MB	Lower 1/4
0	1	1	1	0	0 thru 31	000000h – 1FFFFFFh	2MB	Lower 1/2
X	X	1	1	1	0 thru 63	000000h – 3FFFFFFh	4MB	ALL
1	0	0	0	1	63	3FF000h – 3FFFFFFh	4KB	U - 1/1024
1	0	0	1	0	63	3FE000h – 3FFFFFFh	8KB	U - 1/512
1	0	0	1	1	63	3FC000h – 3FFFFFFh	16KB	U - 1/256
1	0	1	0	X	63	3F8000h – 3FFFFFFh	32KB	U - 1/128
1	1	0	0	1	0	000000h – 00FFFFh	4KB	L - 1/1024
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/512
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/256
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/128

Note:

1. x = don't care
2. L = Lower; U = Upper



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CMP = 1

STATUS REGISTER ⁽¹⁾					W25Q32BV (32M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION ⁽²⁾
X	X	0	0	0	ALL	000000h – 3FFFFFFh	4MB	ALL
0	0	0	0	1	0 thru 62	000000h – 3FFFFFFh	4,032KB	Lower 63/64
0	0	0	1	0	0 and 61	000000h – 3DFFFFh	3,968KB	Lower 31/32
0	0	0	1	1	0 thru 59	000000h – 3BFFFFh	3,840KB	Lower 15/16
0	0	1	0	0	0 thru 55	000000h – 37FFFFh	3,584KB	Lower 7/8
0	0	1	0	1	0 thru 47	000000h – 2FFFFFFh	3MB	Lower 3/4
0	0	1	1	0	0 thru 31	000000h – 1FFFFFFh	2MB	Lower 1/2
0	1	0	0	1	1 thru 63	010000h – 3FFFFFFh	4,032KB	Upper 63/64
0	1	0	1	0	2 and 63	020000h – 3FFFFFFh	3,968KB	Upper 31/32
0	1	0	1	1	4 thru 63	040000h – 3FFFFFFh	3,840KB	Upper 15/16
0	1	1	0	0	8 thru 63	080000h – 3FFFFFFh	3,584KB	Upper 7/8
0	1	1	0	1	16 thru 63	100000h – 3FFFFFFh	3MB	Upper 3/4
0	1	1	1	0	32 thru 63	200000h – 3FFFFFFh	2MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 62	000000h – 3FEFFFh	4,092KB	L - 1023/1024
1	0	0	1	0	0 thru 62	000000h – 3FDFFFh	4,088KB	L - 511/512
1	0	0	1	1	0 thru 62	000000h – 3FBFFFh	4,080KB	L - 255/256
1	0	1	0	X	0 thru 62	000000h – 3F7FFFh	4,064KB	L - 127/128
1	1	0	0	1	1 thru 63	001000h – 3FFFFFFh	4,092KB	U - 1023/1024
1	1	0	1	0	1 thru 63	002000h – 3FFFFFFh	4,088KB	U - 511/512
1	1	0	1	1	1 thru 63	004000h – 3FFFFFFh	4,080KB	U - 255/256
1	1	1	0	X	1 thru 63	008000h – 3FFFFFFh	4,064KB	U - 127/128

Note:

1. x = don't care
2. L = Lower; U = Upper



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4.4 Different RDSR bit definition

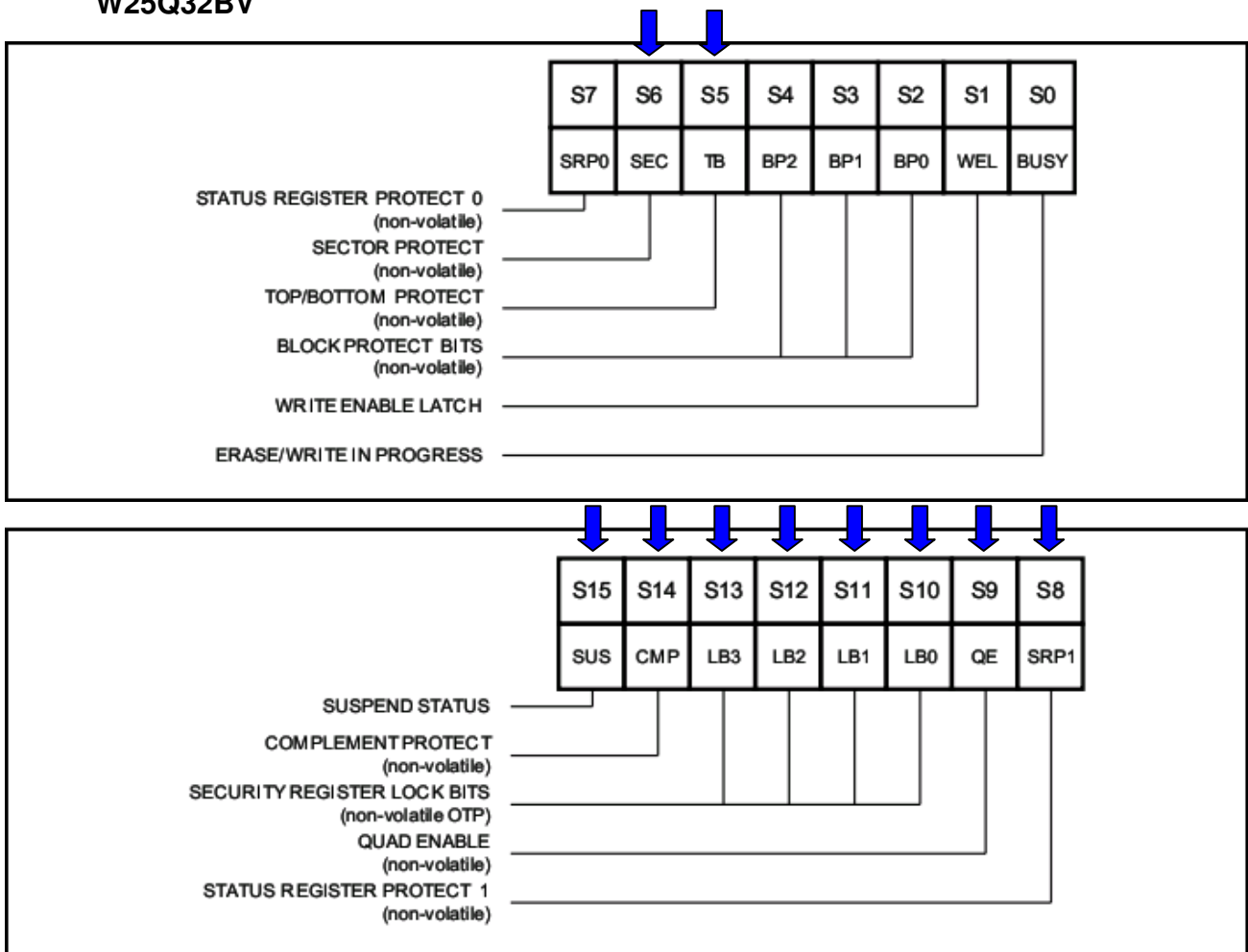
The definition of RDSR bit S5 and S6 are different, and EN25Q32A does not have S8 ~ S15 bits.

EN25Q32B		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

W25Q32BV





5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q32B		W25Q32BV		Unit
	Typ	Max	Typ	Max	
Page programming time	0.8	5	0.7	3	ms
Sector erase time	0.05	0.3	0.03	0.2	sec
Block erase time	0.2	2	0.15	1	sec
Chip (Bulk) erase time	15	25	7	15	sec

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q32B	W25Q32BV
t _{CH} (serial clock high time)	Min @ 4ns	Min @ 6ns
t _{CL} (serial clock low time)	Min @ 4ns	Min @ 6ns
t _{CLCH} (serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t _{CLCL} (serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t _{CHSH} (CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
t _{SHSL} (CS# high time)	Min @ 50ns	Min @ 5ns
t _{DSU} (Data in setup time)	Min @ 2ns	Min @ 1.5ns
t _{DH} (Data in hold time)	Min @ 5ns	Min @ 4ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2010/07/01