



Application Note

EON EN25Q128

VS

MXIC MX25L12845E

Specification Comparison



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from MXIC MX25L12845E Flash to Eon EN25Q128 Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2-1 The following table highlights the major features of these two devices.

| Features | EN25Q128 | MX25L12845E |
|--|---|--|
| Voltage Range | 2.7 ~ 3.6 | 2.7 ~ 3.6 |
| Pin to Pin Compatible (standard SPI mode) | 8-pin VDFN (6x8mm) 16-pins SOP 300mil (except pin 4, 5, 6, 11, 12, 13, 14 = NC) | 8-WSON (6x8mm) 16-pins SOP 300mil (except pin 4, 5, 6 = PO2, PO1, PO0; pin 11, 12, 13, 14 = PO3, PO4, PO5, PO6) |
| SPI frequency | 104MHz (standard mode) 80MHz @ Dual & Quad mode | 104MHz (standard mode) 70MHz @ Dual & Quad mode |
| Secured Silicon Sector Region | 512 Byte | 512 Byte |
| Sector Architecture | Uniform 4096 sectors of 4K byte 256 blocks of 64K byte | Uniform 4096 sectors of 4K byte 512 blocks of 32K byte 256 blocks of 64K byte |
| SPI mode | Mode 0 / Mode 3 | Mode 0 / Mode 3 |
| For Double Transfer Rate serial read mode | No | Yes |
| EQIO mode (Full Quad mode) | Yes | No |
| Page program | Yes | Yes |
| Continuous program | No | Yes |
| Block erase 64K byte | Yes | Yes |
| Block erase 32K Byte | No | Yes |
| Sector erase 4K byte | Yes | Yes |
| Parallel Mode | No | Yes |
| BP table | Enhanced protect (*) | Conventional |
| Advanced individual block protect | No | Yes |
| DMC table | No | Yes |
| Minimum Endurance Cycle | 100K | 100K |
| Package | 8-pin VDFN (5x6mm) 8-pin VDFN (6x8mm) 16-pins SOP 300mil 24-ball BGA (6x8mm) | 8-pins SOP 200mil 8-WSON (6x8mm) 16-pins SOP 300mil |

(*) Please refer to page 5



3. HARDWARE CONSIDERATIONS

3-1 I_{CC} comparison

| Current (Max) | EN25Q128 | MX25L12845E | Unit |
|------------------------------------|---------------------------|---------------------------|------|
| Read I _{CC3} | 25 @ 104MHz 20 @ 80MHz | 45 @ 104MHz 40 @ 70MHz | mA |
| Page Program (PP) I _{CC4} | 28 | 25 | mA |
| Sector Erase (SE) I _{CC6} | 25 | 25 | mA |
| Standby I _{CC1} | 20 | 100 | μA |

3-2 Pin configuration (16-pin package)

| Pin number | EN25Q128 | MX25L12845E |
|------------|-----------|-----------------|
| Pin 1 | NC (DQ3) | NC / SIO3 |
| Pin 2 | VCC | VCC |
| Pin 3 | NC | NC |
| Pin 4 | NC | PO2 |
| Pin 5 | NC | PO1 |
| Pin 6 | NC | PO0 |
| Pin 7 | CS# | CS# |
| Pin 8 | DO (DQ1) | SO / SIO1 / PO7 |
| Pin 9 | WP# (DQ2) | WP# / SIO2 |
| Pin 10 | VSS | GND |
| Pin 11 | NC | PO3 |
| Pin 12 | NC | PO4 |
| Pin 13 | NC | PO5 |
| Pin 14 | NC | PO6 |
| Pin 15 | DI (DQ0) | SI / SIO0 |
| Pin 16 | CLK | SCLK |

Note:

1. Eon EN25Q128 Flash can support the general standard / Dual / Quad SPI mode (Need specific SPI controller), but don't support the Parallel Mode (PO0~PO7).



4. SOFTWARE CONSIDERATIONS

- 4-1 Manufacturer, Memory Type & Device Identification comparison
(M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density)

EN25Q128:

| OP Code | (M7-M0) | (ID15-ID0) | (ID7-ID0) |
|---------|---------|------------|-----------|
| ABh | | | 17h |
| 90h | 1Ch | | 17h |
| 9Fh | 1Ch | 3018h | |

MX25L12845E:

| Command Type | MX25L12845E | | |
|-----------------------------|-----------------|-------------|----------------|
| RDID | manufacturer ID | memory type | memory density |
| | C2 | 20 | 18 |
| RES | electronic ID | | |
| | 17 | | |
| REMS/REMS2/ REMS4/REMS4D | manufacturer ID | device ID | |
| | C2 | 17 | |



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4-2 Instruction Set Comparison

4-2.1 Different block protection area

EN25Q128:

| Status Register Content | | | | Memory Content | | | |
|-------------------------|---------|---------|---------|-----------------|-----------------|-------------|---------------|
| BP3 Bit | BP2 Bit | BP1 Bit | BP0 Bit | Protect Areas | Addresses | Density(KB) | Portion |
| 0 | 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 0 | 1 | Block 0 to 254 | 000000h-FEFFFFh | 16320KB | Lower 255/256 |
| 0 | 0 | 1 | 0 | Block 0 to 253 | 000000h-FDFFFFh | 16256KB | Lower 254/256 |
| 0 | 0 | 1 | 1 | Block 0 to 251 | 000000h-FBFFFFh | 16128KB | Lower 252/256 |
| 0 | 1 | 0 | 0 | Block 0 to 247 | 000000h-F7FFFFh | 15872KB | Lower 248/256 |
| 0 | 1 | 0 | 1 | Block 0 to 239 | 000000h-EFFFFFh | 15360KB | Lower 240/256 |
| 0 | 1 | 1 | 0 | Block 0 to 223 | 000000h-DFFFFFh | 14336KB | Lower 224/256 |
| 0 | 1 | 1 | 1 | All | 000000h-FFFFFFh | 16384KB | All |
| 1 | 0 | 0 | 0 | None | None | None | None |
| 1 | 0 | 0 | 1 | Block 255 to 1 | FFFFFFh-010000h | 16320KB | Upper 255/256 |
| 1 | 0 | 1 | 0 | Block 255 to 2 | FFFFFFh-020000h | 16256KB | Upper 254/256 |
| 1 | 0 | 1 | 1 | Block 255 to 4 | FFFFFFh-040000h | 16128KB | Upper 252/256 |
| 1 | 1 | 0 | 0 | Block 255 to 8 | FFFFFFh-080000h | 15872KB | Upper 248/256 |
| 1 | 1 | 0 | 1 | Block 255 to 16 | FFFFFFh-100000h | 15360KB | Upper 240/256 |
| 1 | 1 | 1 | 0 | Block 255 to 32 | FFFFFFh-200000h | 14336KB | Upper 224/256 |
| 1 | 1 | 1 | 1 | All | FFFFFFh-000000h | 16384KB | All |

MX25L12845E:

| Status bit | | | | Protection Area |
|------------|-----|-----|-----|-----------------------------------|
| BP3 | BP2 | BP1 | BP0 | 128Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (2 blocks, block 254th-255th) |
| 0 | 0 | 1 | 0 | 2 (4 blocks, block 252nd-255th) |
| 0 | 0 | 1 | 1 | 3 (8 blocks, block 248th-255th) |
| 0 | 1 | 0 | 0 | 4 (16 blocks, block 240th-255th) |
| 0 | 1 | 0 | 1 | 5 (32 blocks, block 224th-255th) |
| 0 | 1 | 1 | 0 | 6 (64 blocks, block 192nd-255th) |
| 0 | 1 | 1 | 1 | 7 (128 blocks, block 128th-255th) |
| 1 | 0 | 0 | 0 | 8 (256 blocks, all) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, all) |
| 1 | 0 | 1 | 0 | 10 (256 blocks, all) |
| 1 | 0 | 1 | 1 | 11 (256 blocks, all) |
| 1 | 1 | 0 | 0 | 12 (256 blocks, all) |
| 1 | 1 | 0 | 1 | 13 (256 blocks, all) |
| 1 | 1 | 1 | 0 | 14 (256 blocks, all) |
| 1 | 1 | 1 | 1 | 15 (256 blocks, all) |

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.



4-2.2 Different RDSR bit definition

EN25Q128:

| S7 | | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
|---|-----------------------------------|---|----------------------------------|----------------------------------|----------------------------------|----------------------------------|--|---|
| SRP Status Register Protect | OTP_LOCK bit (note 1) | WPDIS (WP# disable) | BP3 (Block Protected bits) | BP2 (Block Protected bits) | BP1 (Block Protected bits) | BP0 (Block Protected bits) | WEL (Write Enable Latch) | WIP (Write In Progress bit) (Note 3) |
| 1 = status register write disable | 1 = OTP sector is protected | 1 = WP# disable 0 = WP# enable | (note 2) | (note 2) | (note 2) | (note 2) | 1 = write enable 0 = not write enable | 1 = write operation 0 = not in write operation |
| Non-volatile bit | | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

MX25L12845E:

Bit 7 is only used for SRWD (status register write protect).

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|--|---|---|---|---|---|--|---|
| SRWD (status register write protect) | QE (Quad Enable) | BP3 (level of protected block) | BP2 (level of protected block) | BP1 (level of protected block) | BP0 (level of protected block) | WEL (write enable latch) | WIP (write in progress bit) |
| 1=status register write disable | 1= Quad Enable 0=not Quad Enable | (note 1) | (note 1) | (note 1) | (note 1) | 1=write enable 0=not write enable | 1=write operation 0=not in write operation |
| Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

Note 1: see the Table "Protected Area Size"



4-2.3 Security Register definition

EN25Q128: None

MX25L12845E:

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|--|---|---|--|--------------|--------------|--|---|
| WPSEL | E_FAIL | P_FAIL | Continuously Program mode (CP mode) | x | x | LDSO (lock-down 4K-bit Secured OTP) | 4K-bit Secured OTP |
| 0=normal WP mode 1=individual WP mode (default=0) | 0=normal Erase succeed 1=indicate Erase failed (default=0) | 0=normal Program succeed 1=indicate Program failed (default=0) | 0=normal Program mode 1=CP mode (default=0) | reserved | reserved | 0 = not lockdown 1 = lock-down (cannot program/erase OTP) | 0 = nonfactory lock 1 = factory lock |
| non-volatile bit | volatile bit | volatile bit | volatile bit | volatile bit | volatile bit | non-volatile bit | non-volatile bit |
| OTP | Read Only | Read Only | Read Only | Read Only | Read Only | OTP | Read Only |

4-2.4 EQIO mode (Enable Quad I/O) (38h)

EN25Q128: This command will enable device enter Full Quad mode.

MX25L12845E: Only support the page program under Quad mode.

4-2.5 Enter Secured OTP command

EN25Q128: Support. (3Ah)

MX25L12845E: Support. (B1h)

4-2.6 Exit Secured OTP command

EN25Q128: Support. (04h)

MX25L12845E: Support. (C1h)



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4-2.7 Secured OTP Addresses

EN25Q128:

| Sector | Sector Size | Address Range |
|--------|-------------|-------------------|
| 4095 | 512 byte | FFF000h – FFF1FFh |

MX25L12845E:

| Address range | Size | Standard Factory Lock | Customer Lock |
|---------------|----------|--------------------------------|------------------------|
| xxx000~xxx00F | 128-bit | ESN (electrical serial number) | Determined by customer |
| xxx010~xxxFFF | 3968-bit | N/A | |



4-2.8 The other instructions comparison

| Instructions | Command | EN25Q128 | MX25L12845E |
|---|----------------|-----------------|--------------------|
| RSTQIO (Reset Quad I/O) | FFh | Yes | No |
| RSTEN (Reset Enable) | 66h | Yes | No |
| RST (Reset) | 99h | Yes | No |
| Dual Output Fast Read | 3Bh | Yes | No |
| BE 32K (block erase 32KB) | 52h | No | Yes |
| CP (Continuously Program mode) | ADh | No | Yes |
| REMS2 (Read ID for 2x I/O mode) | EFh | No | Yes |
| REMS4 (Read ID for 4x I/O mode) | DFh | No | Yes |
| REMS4D (Read ID for 4 x I/O DT mode) | CFh | No | Yes |
| RDSCUR (Read Security register) | 2Bh | No | Yes |
| WRSCUR (Write Security register) | 2Fh | No | Yes |
| ESRY (Enable SO to output RY/BY#) | 70h | No | Yes |
| DSRY (Disable SO to output RY/BY#) | 80h | No | Yes |
| ENPLM (Enter Parallel Mode) | 55h | No | Yes |
| EXPLM (Exit Parallel Mode) | 45h | No | Yes |
| CLSR (Clear SR Fail Flags) | 30h | No | Yes |
| HPM (High Performance Enable Mode) | A3h | No | Yes |
| WPSEL (write protection selection) | 68h | No | Yes |
| SBLK (single block lock) | 36h | No | Yes |
| SBULK (single block unlock) | 39h | No | Yes |
| RDBLOCK (block protect read) | 3Ch | No | Yes |
| GBLK (gang block lock) | 7Eh | No | Yes |
| GBULK (gang block unlock) | 98h | No | Yes |
| RDDMC (Read DMC) | 5A | No | Yes |



5. PERFORMANCE DIFFERENCES

5-1 Erase and program performance

| Parameter | EN25Q128 | | MX25L12845E | | Unit |
|-------------------------|----------|-----|-------------|-----|------|
| | Typ | Max | Typ | Max | |
| Page Programming Time | 0.8 | 5 | 1.4 | 5 | ms |
| Sector Erase Time | 50 | 300 | 60 | 300 | ms |
| Block Erase Time (32KB) | N/A | N/A | 0.5 | 2 | sec |
| Block Erase Time (64KB) | 0.2 | 2 | 0.7 | 2 | sec |
| Chip (Bulk) Erase Time | 45 | 90 | 80 | 200 | sec |

5-2 Key AC parameter PERFORMANCE

| Parameter | EN25Q128 | MX25L12845E |
|-------------------------------------|--|--|
| tCH (serial clock high time) | Min @ 4ns | Min @ 4.5ns |
| tCL (serial clock low time) | Min @ 4ns | Min @ 4.5ns |
| tCLCH(serial clock rise time) | Min @ 0.1V / ns | Min @ 0.1V / ns |
| tCHCL(serial clock fall time) | Min @ 0.1V / ns | Min @ 0.1V / ns |
| tCHSH(CS# active setup / hold time) | Min@ 5ns | Min @ 5ns |
| tSHSL(CS# high time) | Min, read @15ns Program/Erase @50ns | Min, read @15ns Program/Erase @50ns |
| tDSU(Data in setup time) | Min @ 2ns | Min @ 2ns |
| tDH(Data in hold time) | Min @ 5ns | Min @ 5ns |



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Revisions List

| Revision No | Description | Date |
|-------------|-----------------|------------|
| A | Initial Release | 2010/09/14 |