Application Note

EON	**EN25Q32B**	(Version: A)
	VS.	
SST	**SST25VF032B**	(Version: 03)

1. INTRODUCTION

The application note introduces how to implement a system design from SST flash SST25VF032B to Eon flash EN25Q32B.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1. The following table highlights the major features of these two devices.

Features	EN25Q32B	SST25VF032B
Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Pin to Pin Compatible	Yes	Yes
SPI Mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI Frequency	104MHz (standard mode) 80MHz @ dual & quad mode	80MHz (standard mode)
Sector Architecture	Uniform ● 1024 sectors of 4Kbyte ● 64 blocks of 64Kbyte ● Any sector or block can be erased individually.	Uniform ● 1024 sectors of 4Kbyte ● 64 blocks of 64Kbyte ● Any sector or block can be erased individually.
Lockable OTP Security Sector	512 Bytes	No
HOLD# Pin	No	Yes
Page Programming	Yes	No
Auto Address Increment (AAI) Word Programming	No	Yes
Block Erase 32KBytes	No	Yes
Minimum Endurance Cycle	100K	100K
Package[1.]	8 pins SOP 200mil body width 8 contact VDFN (5x6mm) 16 pins SOP 300mil body width 24 balls BGA (6x8mm) ● All Pb-free packages are RoHS compliant	8 pins SOP 200mil body width 8 pins WSON (5x6mm) ● All Pb-free packages are RoHS compliant

Note:

1. Please refer to the datasheet in detail.

3. HARDWARE CONSIDERATIONS

3.1. I_{CC} Comparison

Current	EN25Q32B	SST25VF032B	Unit
	Max (@ Single 104MHz)	Max (@ 80MHz)	
Read I_{CC3}	25	25	mA
Page Program (PP) I_{CC4}	28	30	mA
Sector Erase (SE) I_{CC6}	25	30	mA
Standby I_{CC1}	20	20	μA

3.2. Pins Description

EN25Q32B		SST25VF032B	
Pin Name	Function	Pin Name	Function
CLK	Serial Clock Input	SCK	Serial Clock Input
DI (DQ0)	Serial Data Input (Data Input Output 0) *1	SI	Serial Data Input
DO (DQ1)	Serial Data Output (Data Input Output 1) *1	SO (RY/BY#)	Serial Data Output (Flash busy status pin in AAI mode if SO is configured as a hardware RY/BY# pin)
CS#	Chip Enable	CS#	Chip Enable
WP# (DQ2)	Write Protect (Data Input Output 2) *2	WP#	Write Protect
NC(DQ3)	Not Connect (Data Input Output 3) *2	HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)	VDD	Supply Voltage (2.7-3.6V)
Vss	Ground	Vss	Ground
NC	No Connect	NC	No Connect

Note:

1. DQ0 and DQ1 are used for Dual and Quad instructions.

2. DQ0 ~ DQ3 are used for Quad instructions.

* Users must take care of the different pin definition!

4. SOFTWARE CONSIDERATIONS

4.1. Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

4.1.1. For **EN25Q32B**：MANUFACTURER/DEVICE ID TABLE

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			15h
90h	1Ch		15h
9Fh	1Ch	3016h	

4.1.2. For **SST25VF032B**：MANUFACTURER/DEVICE ID TABLE

JEDEC Read-ID Data

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	4AH

4.2. Instruction Set Comparison

4.2.1. For **EN25Q32B**：Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQIO	38h						
RSTQIO(2) / Release Quad I/O or Fast Read Enhanced Mode	FFh						
RSTEN	66h						
RST(1)	99h						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0)(3)					continuous(4)
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(5)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(6)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		
Enter OTP mode	3Ah						

Notes:
1. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
2. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
4. The Status Register contents will repeat continuously until CS# terminates the instruction.
5. The Device ID will repeat continuously until CS# terminates the instruction.
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
7. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.

Instruction Set (Read Instruction)

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …) (1)	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8(2)	A7-A0, dummy (2)	(D7-D0, …) (1)			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh	A23-A0, dummy (4)	(dummy, D7-D0) (5)	(D7-D0, …) (3)			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data

DQ_0 = (D6, D4, D2, D0)

DQ_1 = (D7, D5, D3, D1)

2. Dual Input Address

DQ0 = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, dummy 6, dummy 4, dummy 2, dummy 0

DQ1 = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, dummy 7, dummy 5, dummy 3, dummy 1

3. Quad Data

DQ0 = (D4, D0, ……)

DQ1 = (D5, D1, ……)

DQ2 = (D6, D2, ...)

DQ3 = (D7, D3, ...)

4. Quad Input Address

DQ0 = A20, A16, A12, A8, A4, A0, dummy 4, dummy 0

DQ1 = A21, A17, A13, A9, A5, A1, dummy 5, dummy 1

DQ2 = A22, A18, A14, A10, A6, A2, dummy 6, dummy 2

DQ3 = A23, A19, A15, A11, A7, A3, dummy 7, dummy 3

5. Quad I/O Fast Read Data

DQ0 = (dummy 12, dummy 8, dummy 4, dummy 0, D4, D0)

DQ1 = (dummy 13, dummy 9, dummy 5, dummy 1, D5, D1)

DQ2 = (dummy 14, dummy 10, dummy 6, dummy 2, D6, D2)

DQ3 = (dummy 15, dummy 11, dummy 7, dummy 3, D7, D3)

4.2.2. For **SST25VF032B**：Instruction Set

Device Operation Instructions

Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	25 MHz
High-Speed Read	Read Memory at higher speed	0000 1011b (0BH)	3	1	1 to ∞	80 MHz
4 KByte Sector-Erase[3]	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0	80 MHz
32 KByte Block-Erase[4]	Erase 32KByte block of memory array	0101 0010b (52H)	3	0	0	80 MHz
64 KByte Block-Erase[5]	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0	80 MHz
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	80 MHz
Byte-Program	To Program One Data Byte	0000 0010b (02H)	3	0	1	80 MHz
AAI-Word-Program[6]	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞	80 MHz
RDSR[7]	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞	80 MHz
EWSR	Enable-Write-Status-Register	0101 0000b (50H)	0	0	0	80 MHz
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1	80 MHz
WREN	Write-Enable	0000 0110b (06H)	0	0	0	80 MHz
WRDI	Write-Disable	0000 0100b (04H)	0	0	0	80 MHz
RDID[8]	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞	80 MHz
JEDEC-ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞	80 MHz
EBSY	Enable SO as an output RY/BY# status during AAI programming	0111 0000b (70H)	0	0	0	80 MHz
DBSY	Disable SO as an output RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0	80 MHz

1. One bus cycle is eight clock periods.
2. Address bits above the most significant bit can be either V_{IL} or V_{IH}.
3. 4KByte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
4. 32KByte Block Erase addresses: use A_{MS}-A_{15}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
5. 64KByte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
6. To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address [A_{23}-A_1] with A_0=0, Data Byte 1 will be programmed into the initial address [A_{23}-A_1] with A_0 = 1.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
8. Manufacturer's ID is read with A_0 = 0, and Device ID is read with A_0 = 1. All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.

Note:

1. The major differences are pointed out by the blue arrows. Please refer to the datasheet in detail.
2. Users must modify the codes for EN25Q32B!

4.3. Different Block Protection Area

*The definitions of Block Protection Area are different!

4.3.1. For **EN25Q32B** :

Protected Area Sizes Sector Organization Table

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 62	000000h-3EFFFFh	4032KB	Lower 63/64
0	0	1	0	Block 0 to 61	000000h-3DFFFFh	3968KB	Lower 62/64
0	0	1	1	Block 0 to 59	000000h-3BFFFFh	3840KB	Lower 60/64
0	1	0	0	Block 0 to 55	000000h-37FFFFh	3584KB	Lower 56/64
0	1	0	1	Block 0 to 47	000000h-2FFFFFh	3072KB	Lower 48/64
0	1	1	0	Block 0 to 31	000000h-1FFFFFh	2048KB	Lower 32/64
0	1	1	1	All	000000h-3FFFFFh	4096KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 63 to 1	3FFFFFh-010000h	4032KB	Upper 63/64
1	0	1	0	Block 63 to 2	3FFFFFh-020000h	3968KB	Upper 62/64
1	0	1	1	Block 63 to 4	3FFFFFh-040000h	3840KB	Upper 60/64
1	1	0	0	Block 63 to 8	3FFFFFh-080000h	3584KB	Upper 56/64
1	1	0	1	Block 63 to 16	3FFFFFh-100000h	3072KB	Upper 48/64
1	1	1	0	Block 63 to 32	3FFFFFh-200000h	2048KB	Upper 32/64
1	1	1	1	All	000000h-3FFFFFh	4096KB	All

4.3.2. For **SST25VF032B** :

Software Status Register Block Protection FOR SST25VF032B[1]

	Status Register Bit[2]				Protected Memory Address
Protection Level	BP3	BP2	BP1	BP0	32 Mbit
None	X	0	0	0	None
Upper 1/64	X	0	0	1	3F0000H-3FFFFFH
Upper 1/32	X	0	1	0	3E0000H-3FFFFFH
Upper 1/16	X	0	1	1	3C0000H-3FFFFFH
Upper 1/8	X	1	0	0	380000H-3FFFFFH
Upper 1/4	X	1	0	1	300000H-3FFFFFH
Upper 1/2	X	1	1	0	200000H-3FFFFFH
All Blocks	X	1	1	1	000000H-3FFFFFH

T4.0 1327

1. X = Don't Care (RESERVED) default is "0
2. Default at power-up for BP2, BP1, and BP0 is '111'. (All Blocks Protected)

4.4. Different RDSR Bits Definition

*The definitions of RDSR bits [S7:S6] are different!

4.4.1. For **EN25Q32B** :

Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table “Protected Area Sizes Sector Organization”.

4.4.2. For **SST25VF032B** :

Software Status Register

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 4)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 4)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 4)	1	R/W
5	BP3	Indicate current level of block write protection (See Table 4)	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are readable/writable	0	R/W

4.5. Different One Time Programming Definition

*The definitions of OTP are different!

4.5.1. For **EN25Q32B**：

OTP Sector Address

Sector	Sector Size	Address Range
1023	512 Bytes	3FF000h – 3FF1FFh

Note: The OTP sector is mapping to sector 1023

4.5.2. For **SST25VF032B**：NO

5. PERFORMANCE DIFFERENCES

5.1. KEY AC PARAMETER PERFORMANCE

Parameter		EN25Q32B	SST25VF032B
t_{CH} (serial clock high time)		Min @ 4ns	Min @ 6ns
t_{CL} (serial clock low time)		Min @ 4ns	Min @ 6ns
t_{CLCH}(serial clock rise time)		Min @ 0.1V / ns	Min @ 0.1V / ns
t_{CLCL}(serial clock fall time)		Min @ 0.1V / ns	Min @ 0.1V / ns
t_{CHSH}(CS# active setup / hold time)		Min@ 5ns	Min @ 5ns
t_{SHSL}	(CS# high time for read) (CS# high time for program/erase)	Min @ 15ns Min @ 50ns	Min @ 50ns
t_{DSU}(Data in setup time)		Min @ 2ns	Min @ 2ns
t_{DH}(Data in hold time)		Min @ 5ns	Min @ 4ns

5.2. Power-On Timings

Parameter	Description	EN25Q32B	SST25VF032B
t_{VSL}	V_{CC}(min) to CS# low	10µs	
t_{PUW}	Time delay to Write instruction	10ms	
$t_{PU-READ}$ $t_{PU-WRITE}$	V_{DD} Min to Read/Write Operation		100µs

5.3. ERASE AND PROGRAM PERFORMANCE

The ERASE and PROGRAM Performance Comparison

Parameter	EN25Q32B		SST25VF032B		Unit
	Typ	Max	Typ	Max	
Page Programming Time	0.8ms	5ms		10µs[*1]	
Sector Erase Time	0.05	0.3		0.025	sec
Block Erase Time	0.2	2		0.025	sec
Chip Erase Time	15	25		0.05	sec

Note:

1. For one byte programming time.

Revisions List

Revision No	Description	Date
A	Initial Release	2010/12/29