



Purpose

Eon Silicon Solution Inc. (hereinafter called "Eon") is going to provide its products' top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon's product family.

Eon products' New Top Marking

cFeon

cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX

Lot Number: XXXXX

Date Code: XXXXX

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as an Eon product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

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For More Information

Please contact your local sales office for additional information about Eon memory solutions.

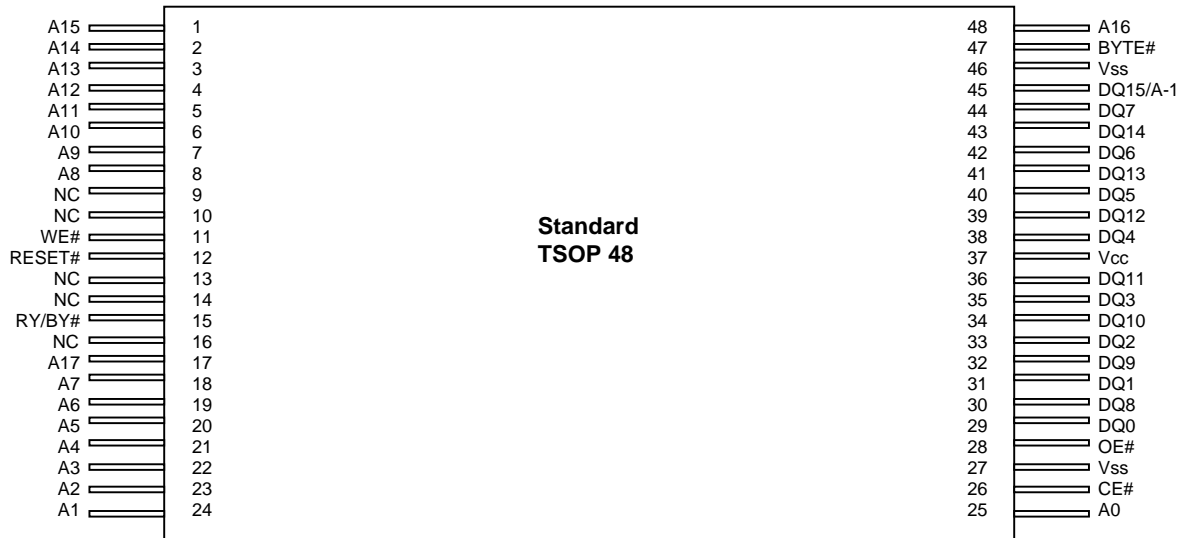
**EN29LV400A****4 Megabit (512K x 8-bit / 256K x 16-bit) Flash Memory
Boot Sector Flash Memory, CMOS 3.0 Volt-only****FEATURES**

- 3V, single power supply operation
 - Full voltage range: 2.7-3.6 volt read and write operations for battery-powered applications.
 - Regulated voltage range: 3.0-3.6 volt read and write operations for compatibility with high performance 3.3 volt microprocessors.
- High performance
 - Access times as fast as 45 ns
- Low power consumption (typical values at 5 MHz)
 - 7 mA typical active read current
 - 15 mA typical program/erase current
 - 1 μ A typical standby current (standard access time to active mode)
- Flexible Sector Architecture:
 - One 16 K-byte, two 8 K-byte, one 32 K-byte, and seven 64 K-byte sectors (byte mode)
 - One 8 K-word, two 4 K-word, one 16 K-word and seven 32 K-word sectors (word mode)
- Sector protection:
 - Hardware locking of sectors to prevent program or erase operations within individual sectors
 - Additionally, temporary Sector Unprotect allows code changes in previously locked sectors.
- High performance program/erase speed
 - Byte/Word program time: 8 μ s typical
 - Sector erase time: 500ms typical
- JEDEC Standard Embedded Erase and Program Algorithms
- JEDEC standard DATA# polling and toggle bits feature
- Single Sector and Chip Erase
- Sector Unprotect Mode
- Erase Suspend / Resume modes:
Read or program another Sector during Erase Suspend Mode
- triple-metal double-poly triple-well CMOS Flash Technology
- Low Vcc write inhibit \leq 2.5V
- minimum 100K program/erase endurance cycle
- Package Options
 - 48-pin TSOP (Type 1)
 - 48-ball 6mm x 8mm TFBGA
 - 48-ball 4mm x 6mm WFBGA
- Commercial and Industrial Temperature Range

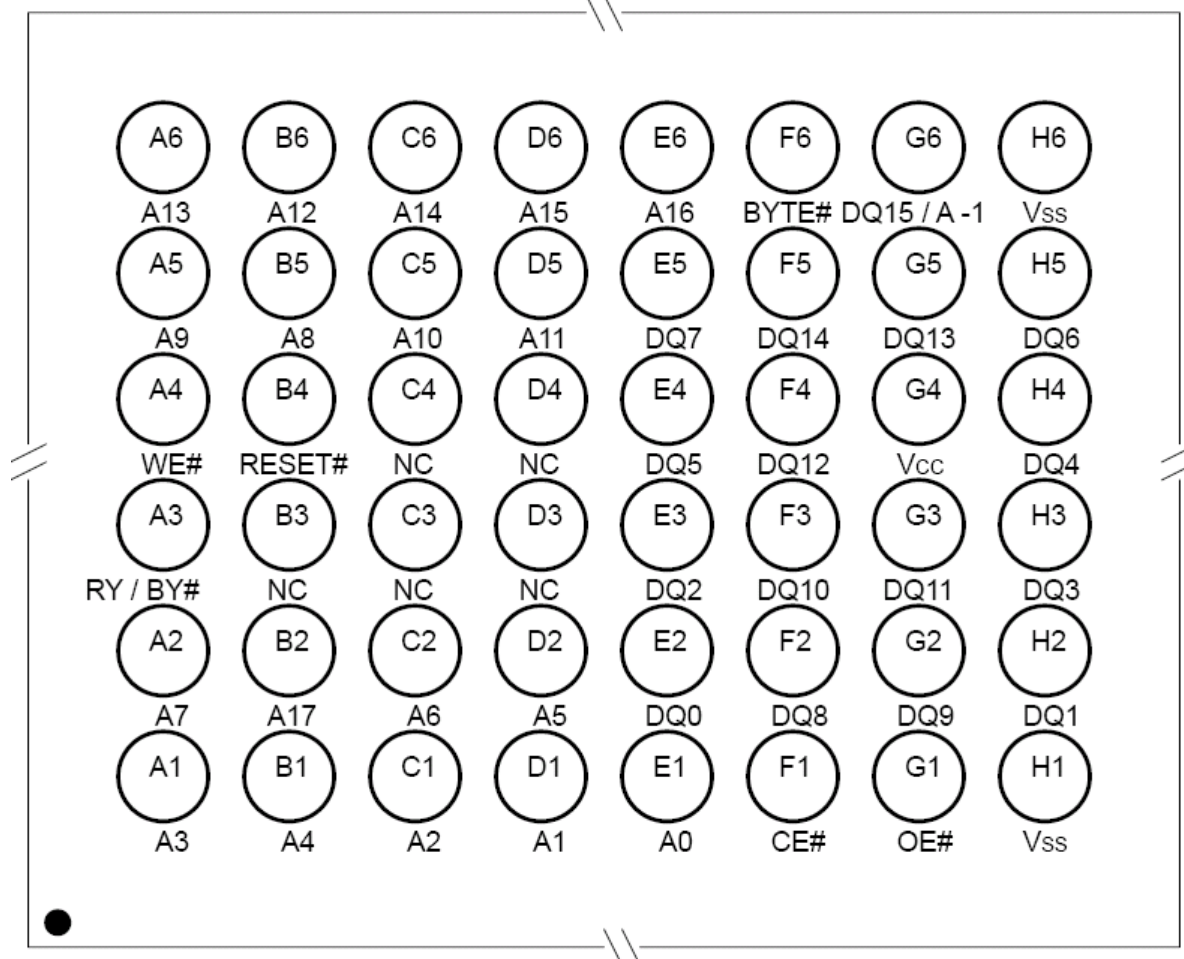
GENERAL DESCRIPTION

The EN29LV400A is a 4-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 524,288 bytes or 256,144 words. Any byte can be programmed typically in 8 μ s. The EN29LV400A features 3.0V voltage read and write operation, with access times as fast as 45ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29LV400A has separate Output Enable (OE#), Chip Enable (CE#), and Write Enable (WE#) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

CONNECTION DIAGRAMS


48-Ball TFBGA
Top View, Balls Facing Down



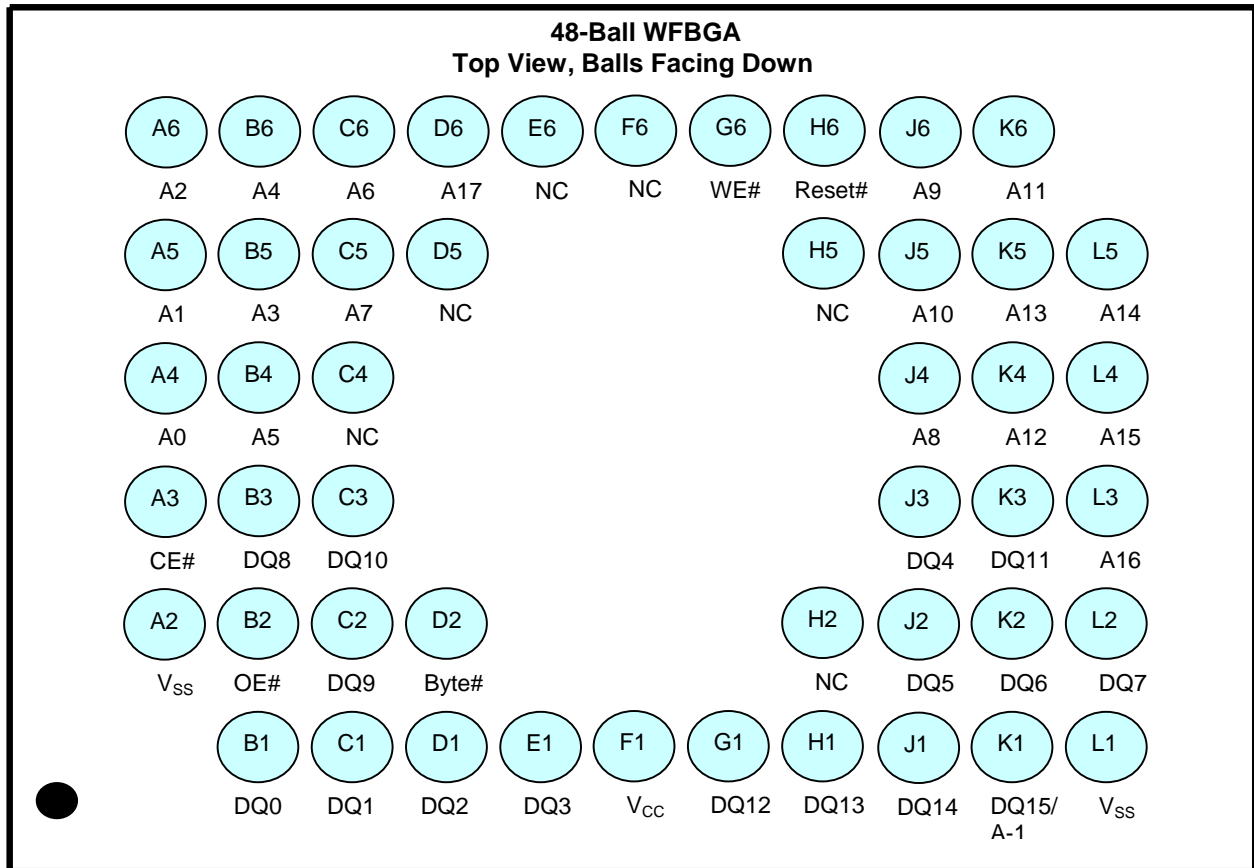


TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A17	Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable
OE#	Output Enable
RESET#	Hardware Reset Pin
RY/BY#	Ready/Busy Output
WE#	Write Enable
Vcc	Supply Voltage
Vss	Ground
NC	Not Connected to anything
BYTE#	Byte/Word Mode

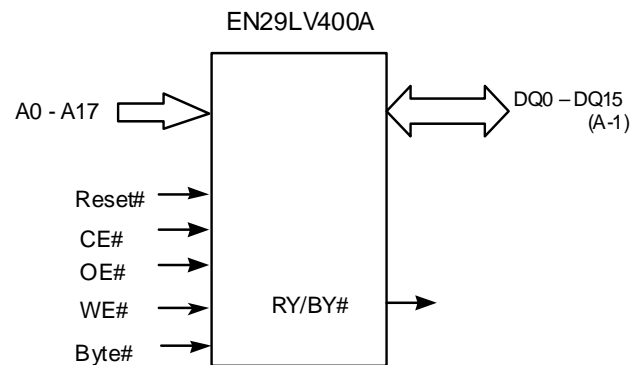
FIGURE 1. LOGIC DIAGRAM




TABLE 2A. TOP BOOT BLOCK SECTOR ARCHITECTURE

Sector	ADDRESS RANGE		SECTOR SIZE (Kbytes / Kwords)	A17	A16	A15	A14	A13	A12
	(X16)	(X8)							
10	3E000h-3FFFFh	7C000h-7FFFFh	16/8	1	1	1	1	1	X
9	3D000h-3DFFFh	7A000h-7BFFFh	8/4	1	1	1	1	0	1
8	3C000h-3CFFFh	78000h-79FFFh	8/4	1	1	1	1	0	0
7	38000h-3BFFFh	70000h – 77FFFh	32/16	1	1	1	0	X	X
6	30000h-37FFFh	60000h - 6FFFFh	64/32	1	1	0	X	X	X
5	28000h-2FFFFh	50000h – 5FFFFh	64/32	1	0	1	X	X	X
4	20000h-27FFFh	40000h – 4FFFFh	64/32	1	0	0	X	X	X
3	18000h-1FFFFh	30000h – 3FFFFh	64/32	0	1	1	X	X	X
2	10000h-17FFFh	20000h - 2FFFFh	64/32	0	1	0	X	X	X
1	08000h-0FFFFh	10000h - 1FFFFh	64/32	0	0	1	X	X	X
0	00000h-07FFFh	00000h - 0FFFFh	64/32	0	0	0	X	X	X



TABLE 2B. BOTTOM BOOT BLOCK SECTOR ARCHITECTURE

Sector	ADDRESS RANGE		SECTOR SIZE (Kbytes/ Kwords)	A17	A16	A15	A14	A13	A12
	(X16)	(X8)							
10	38000h-3FFFFh	70000h – 7FFFFh	64/32	1	1	1	X	X	X
9	30000h-37FFFh	60000h – 6FFFFh	64/32	1	1	0	X	X	X
8	28000h-2FFFFh	50000h – 5FFFFh	64/32	1	0	1	X	X	X
7	20000h-27FFFh	40000h – 4FFFFh	64/32	1	0	0	X	X	X
6	18000h-1FFFFh	30000h – 3FFFFh	64/32	0	1	1	X	X	X
5	10000h-17FFFh	20000h – 2FFFFh	64/32	0	1	0	X	X	X
4	08000h-0FFFFh	10000h – 1FFFFh	64/32	0	0	1	X	X	X
3	04000h-07FFFh	08000h – 0FFFFh	32/16	0	0	0	1	X	X
2	03000h-03FFFh	06000h – 07FFFh	8/4	0	0	0	0	1	1
1	02000h-02FFFh	04000h – 05FFFh	8/4	0	0	0	0	1	0
0	00000h-01FFFh	00000h – 03FFFh	16/8	0	0	0	0	0	X



PRODUCT SELECTOR GUIDE

Product Number		EN29LV400A		
Speed Option	Regulated Voltage Range: Vcc=3.0-3.6 V	-45R	-55R	-70
	Full Voltage Range: Vcc=2.7 – 3.6 V			
Max Access Time, ns (t _{acc})		45	55	70
Max CE# Access, ns (t _{ce})		45	55	70
Max OE# Access, ns (t _{oe})		25	30	30

BLOCK DIAGRAM

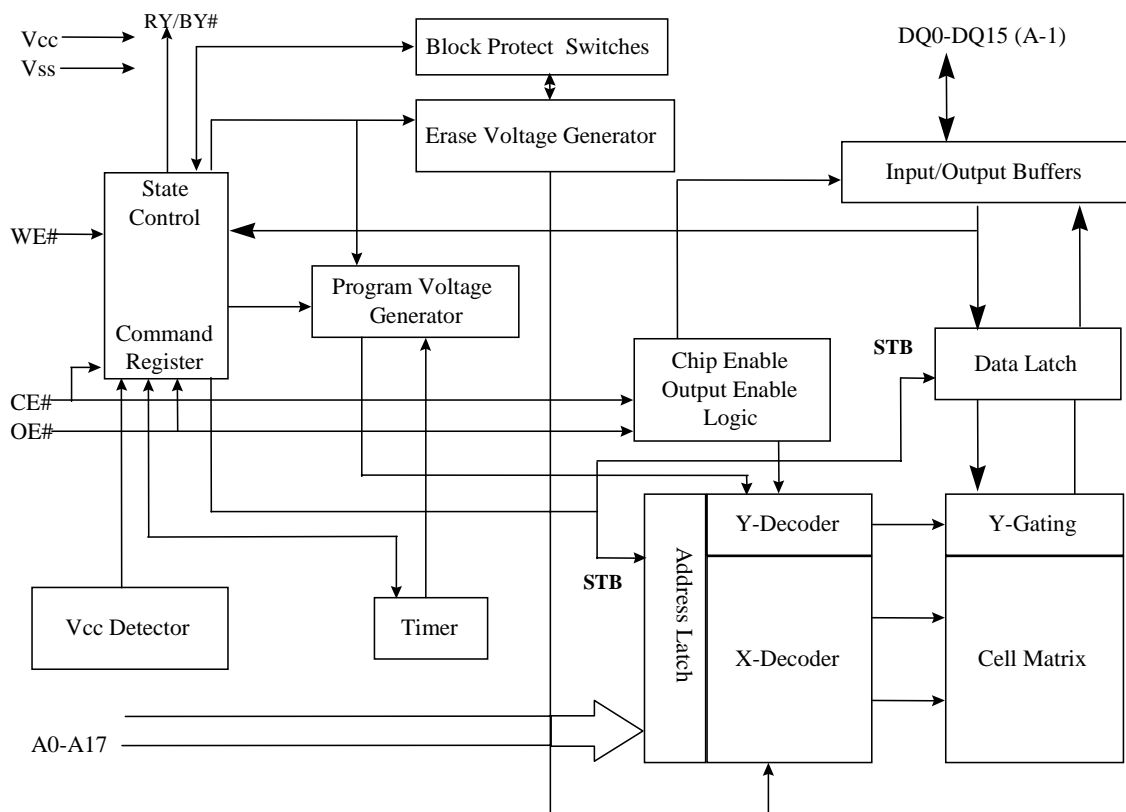




TABLE 3. OPERATING MODES

4M FLASH USER MODE TABLE

Operation	CE#	OE#	WE#	Reset#	A0-A17	DQ0-DQ7	DQ8-DQ15	
							Byte# = V _{IH}	Byte# = V _{IL}
Read	L	L	H	H	A _{IN}	D _{OUT}	D _{OUT}	High-Z
Write	L	H	L	H	A _{IN}	D _{IN}	D _{IN}	High-Z
CMOS Standby	V _{CC} ± 0.3V	X	X	V _{CC} ± 0.3V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect	X	X	X	V _{ID}	A _{IN}	D _{IN}	D _{IN}	X

Notes:

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} =11 ± 0.5V, X=Don't Care (either L or H, but not floating!),
D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In

TABLE 4. DEVICE IDENTIFICATION (Autoselect Codes)

4M FLASH MANUFACTURER/DEVICE ID TABLE

Description	Mode	CE#	OE#	WE#	A17 to A12	A11 to A10	A9 ²	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Eon		L	L	H	X	X	V _{ID}	H ¹ L	X	L	X	L	L	X	1Ch 7Fh
	Device ID (top boot block)	Word	L	L	H	X	X	V _{ID}	X	X	L	X	L	H	22h B9h
Device ID (bottom boot block)	Byte	L	L	H	X	X	V _{ID}	X	X	L	X	L	H	X	B9h
	Word	L	L	H	X	X	V _{ID}	X	X	L	X	L	H	X	22h BAh
Sector Protection Verification	Byte	L	L	H	SA	X	V _{ID}	X	X	L	X	H	L	X	01h (Protected)
	Word	L	L	H	SA	X	V _{ID}	X	X	L	X	H	L	X	00h (Unprotected)

Note:

1. A8 = H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ V_{CC} (CMOS logic level) for Command Autoselect Mode.



USER MODE DEFINITIONS

Word / Byte Configuration

The signal set on the BYTE# Pin controls whether the device data I/O pins DQ15-DQ0 operate in the byte or word configuration. When the Byte# Pin is set at logic '1', then the device is in word configuration, DQ15-DQ0 are active and are controlled by CE# and OE#.

On the other hand, if the Byte# Pin is set at logic '0', then the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Standby Mode

The EN29LV400A has a CMOS-compatible standby mode, which reduces the current to $< 1\mu\text{A}$ (typical). It is placed in CMOS-compatible standby when the CE# pin is at $V_{CC} \pm 0.5$. RESET# and BYTE# pin must also be at CMOS input levels. The device also has a TTL-compatible standby mode, which reduces the maximum V_{CC} current to $< 1\text{mA}$. It is placed in TTL-compatible standby when the CE# pin is at V_{IH} . When in standby modes, the outputs are in a high-impedance state independent of the OE# input.

Read Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" additional details.

Output Disable Mode

When the OE# pin is at a logic high level (V_{IH}), the output from the EN29LV400A is disabled. The output pins are placed in a high impedance state.

Auto Select Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15-DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (10.5V to 11.5 V) on address pin A9. Address pins A8, A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15-DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID} . See "Command Definitions" for details on using the autoselect mode.



Write Mode

Write operations, including programming data and erasing sectors of memory, require the host system to write a command or command sequence to the device. Write cycles are initiated by placing the byte or word address on the device's address inputs while the data to be written is input on DQ[7:0] in Byte Mode (BYTE# = L) or on DQ[15:0] in Word Mode (BYTE# = H). The host system must drive the CE# and WE# pins Low and the OE# pin high for a valid write operation to take place. All addresses are latched on the falling edge of WE# and CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. The system is not required to provide further controls or timings. The device automatically provides internally generated program / erase pulses and verifies the programmed / erased cells' margin. The host system can detect completion of a program or erase operation by observing the RY/BY# pin, or by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits.

The 'Command Definitions' section of this document provides details on the specific device commands implemented in the EN29LV400A.

Sector Protection/Unprotection

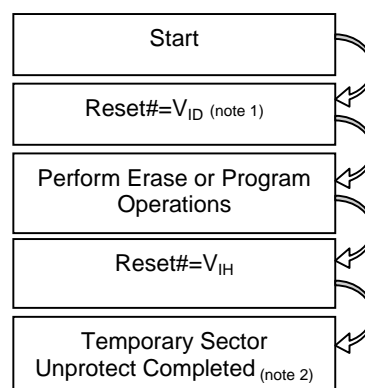
The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

There are two methods to enabling this hardware protection circuitry. The first one requires only that the RESET# pin be at V_{ID} and then standard microprocessor timings can be used to enable or disable this feature. See Flowchart 7a and 7b for the algorithm and Figure 12 for the timings. When doing Sector Unprotect, all the other sectors should be protected first.

The second method is meant for programming equipment. This method requires V_{ID} be applied to both OE# and A9 pin and non-standard microprocessor timings are used. This method is described in a separate document called EN29LV400A Supplement, which can be obtained by contacting a representative of Eon Silicon Devices, Inc.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data while in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by simply selecting the sector addresses. Once is removed from the RESET# pin, all the previously protected sectors are protected again. See accompanying figure and timing diagrams for more details.



- Notes:
1. All protected sectors unprotected.
 2. Previously protected sectors protected again.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{acc} + 30ns. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output is latched and always available to the system. ICC₄ in the DC Characteristics table represents the automatic sleep more current specification.



Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during V_{CC} power up and power down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO} , the device does not accept any write cycles. This protects data during V_{CC} power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO} . The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO} .

Write Pulse “Glitch” protection

Noise pulses of less than 5 ns (typical) on $OE\#$, $CE\#$ or $WE\#$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $OE\# = V_{IL}$, $CE\# = V_{IH}$, or $WE\# = V_{IH}$. To initiate a write cycle, $CE\#$ and $WE\#$ must be a logical zero while $OE\#$ is a logical one. If $CE\#$, $WE\#$, and $OE\#$ are all logical zero (not recommended usage), it will be considered a read.

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with $CE\# = V_{IL}$, $WE\# = V_{IL}$ and $OE\# = V_{IH}$, the device will not accept commands on the rising edge of $WE\#$.



COMMAND DEFINITIONS

The operations of the EN29LV400A are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Sector Protection, Program, Sector Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 5). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

Table 5. EN29LV400A Command Definitions

Command Sequence		Cycles	Bus Cycles														
			1 st Cycle		2 nd Cycle		3 rd Cycle		4 th Cycle		5 th Cycle		6 th Cycle				
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data			
Read		1	RA	RD													
Reset		1	xxx	F0													
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F						
		Byte		AAA		555		AAA		100	1C						000
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	X01	22B9						
		Byte		AAA		555		AAA		X02	B9						
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	X01	22BA						
		Byte		AAA		555		AAA		X02	BA						
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA)	XX00						
		Byte		AAA		555		AAA		X02	XX01						
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD						
		Byte		AAA		555		AAA									
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	AAA	10	
		Byte		AAA		555		AAA		555	55						
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
		Byte		AAA		555		AAA		555	55						
Erase Suspend			1	xxx	B0												
Erase Resume			1	xxx	30												

Address and Data values indicated in hex

RA = Read Address: address of the memory location to be read. This is a read cycle.

RD = Read Data: data read from location RA during Read operation. This is a read cycle.

PA = Program Address: address of the memory location to be programmed. X = Don't-Care

PD = Program Data: data to be programmed at location PA

SA = Sector Address: address of the Sector to be erased or verified. Address bits A17-A12 uniquely select any Sector.

Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following an Erase Suspend command, Erase Suspend mode is entered. The system can read array data using the standard read timings, with the only difference in that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See next section for details on Reset.



Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires V_{ID} on address bit A9 and is intended for PROM programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 4 any number of times, without needing another command sequence.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Word / Byte Programming Command

The device may be programmed by byte or by word, depending on the state of the Byte# Pin. Programming the EN29LV400A is performed by using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of CE# or WE#, whichever is last; data is latched on the rising edge of CE# or WE#, whichever is first.

Programming status may be checked by sampling data on DQ7 (DATA# polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a 0 to a 1. Only an erase operation can change a data from 0 to 1. When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.



The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Flowchart 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend / Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don't-cares when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 μ s to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Erase Suspend Mode.

The system must write the Erase Resume command (address bits are don't-care) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



WRITE OPERATION STATUS

DQ7: DATA# Polling

The EN29LV400A provides DATA# polling on DQ7 to indicate the status of the embedded operations. The DATA# polling feature is active during the embedded Programming, Sector Erase, Chip Erase, and Erase Suspend. (See Table 6)

When the embedded Programming is in progress, an attempt to read the device will produce the complement of the data written to DQ7. Upon the completion of the embedded Programming, an attempt to read the device will produce the true data written to DQ7. For the embedded Programming, DATA# polling is valid after the rising edge of the fourth WE# or CE# pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a “0” at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the “1” at the DQ7 output during the read cycles. For Chip Erase, the DATA# polling is valid after the rising edge of the sixth WE# or CE# pulse in the six-cycle sequence. DATA# polling is valid after the last rising edge of WE# or CE# pulse for chip erase or sector erase.

DATA# Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, DATA# polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable (OE#) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for DATA# polling (DQ7) is shown on Flowchart 5. The DATA# polling (DQ7) timing diagram is shown in Figure 8.

RY/BY#: Ready/Busy Status output

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or completed. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to Vcc.

In the output-low period, signifying Busy, the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high, signifying the Ready, the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

DQ6: Toggle Bit I

The EN29LV400A provides a “Toggle Bit” on DQ6 to indicate the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by active OE# and CE#) will result in DQ6 toggling between “zero” and “one”. Once the embedded Program or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During embedded Programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four-cycle sequence. During Erase operation, the Toggle Bit is valid after the rising edge of the sixth WE# pulses for sector erase or chip erase.



In embedded Programming, if the sector being written to is protected, DQ6 will toggle for about 2 μ s, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected sectors are protected, DQ6 will toggle for about 100 μ s. The chip will then return to the read mode without changing data in all protected sectors.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a “1” on DQ5.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.” Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be used to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from “0” to “1.” This device does not support multiple sector erase command sequences so it is not very meaningful since it immediately shows as a “1” after the first 30h command. Future devices may support this feature.

DQ2: Erase Toggle Bit II

The “Toggle Bit” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to the following table to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.



However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Flowchart 6).

Write Operation Status

Operation		DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A	0



Table 6. Status Register Bits

DQ	Name	Logic Level	Definition
7	DATA# POLLING	'1'	Erase Complete or erase Sector in Erase suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erase Sector during Erase Suspend
		DQ7#	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	TIME OUT BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	ERASE TIME OUT BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase suspend on currently addressed Sector. (When DQ5=1, Erase Error due to currently addressed Sector. Program during Erase Suspend on-going at current address)
		DQ2	Erase Suspend read on non Erase Suspend Sector

Notes:

DQ7 DATA# Polling: indicates the P/E C status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6 Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

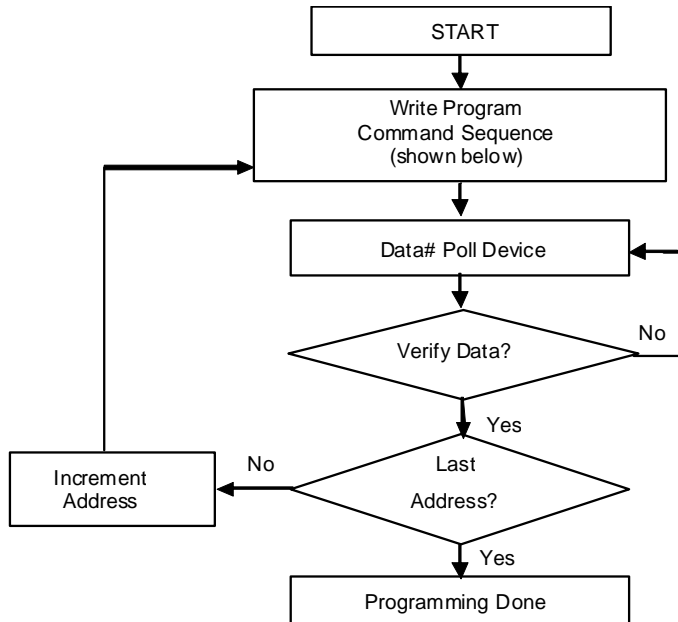
DQ5 Tim Out Bit: set to "1" if failure in programming or erase

DQ3 Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2 Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

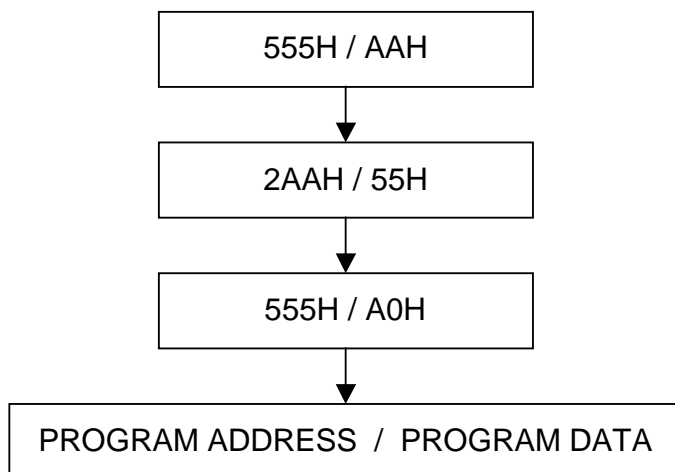
EMBEDDED ALGORITHMS

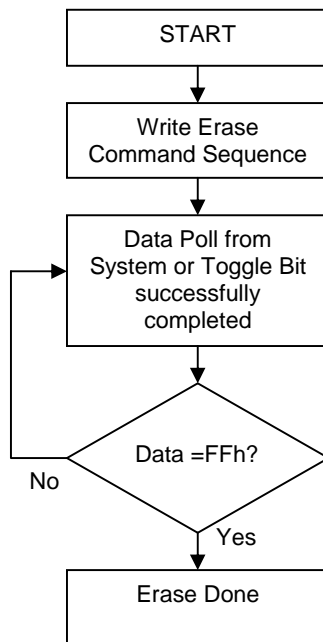
Flowchart 1. Embedded Program



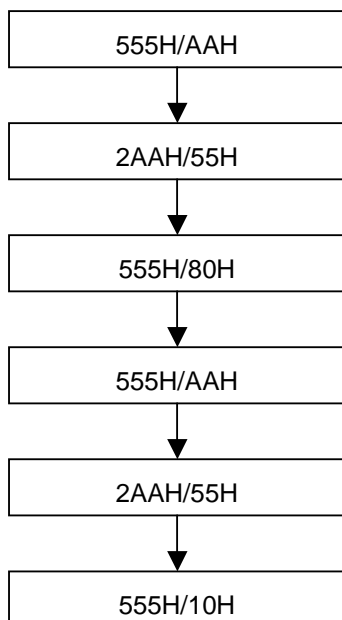
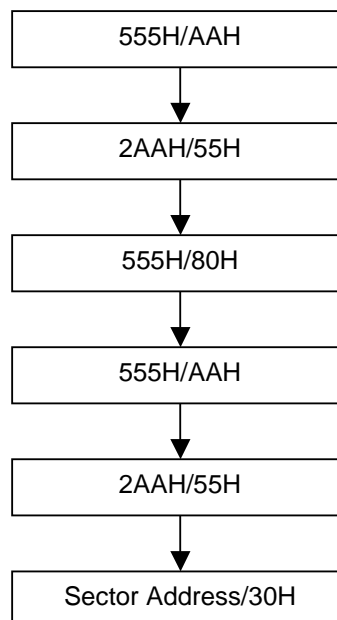
Flowchart 2. Embedded Program Command Sequence

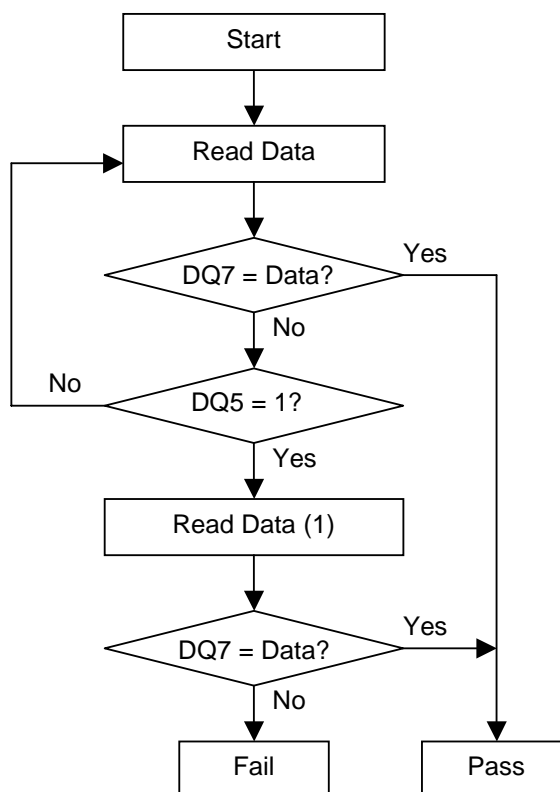
See the Command Definitions section for more information on WORD mode.



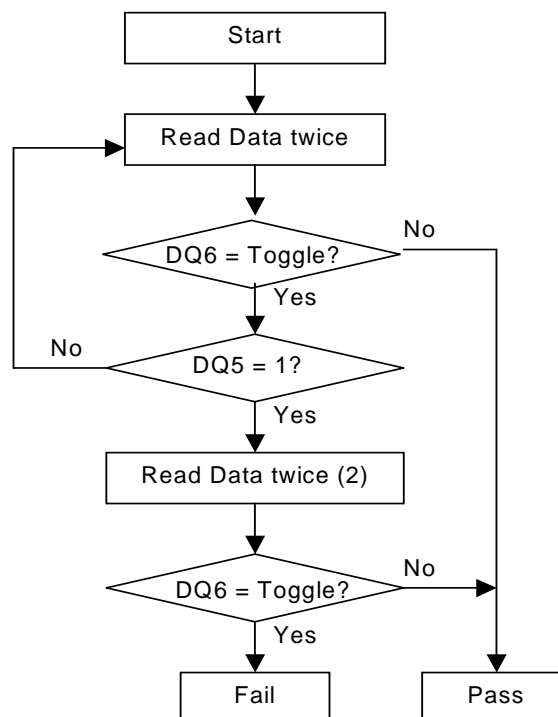
Flowchart 3. Embedded Erase

Flowchart 4. Embedded Erase Command Sequence

See the Command Definitions section for more information on WORD mode.

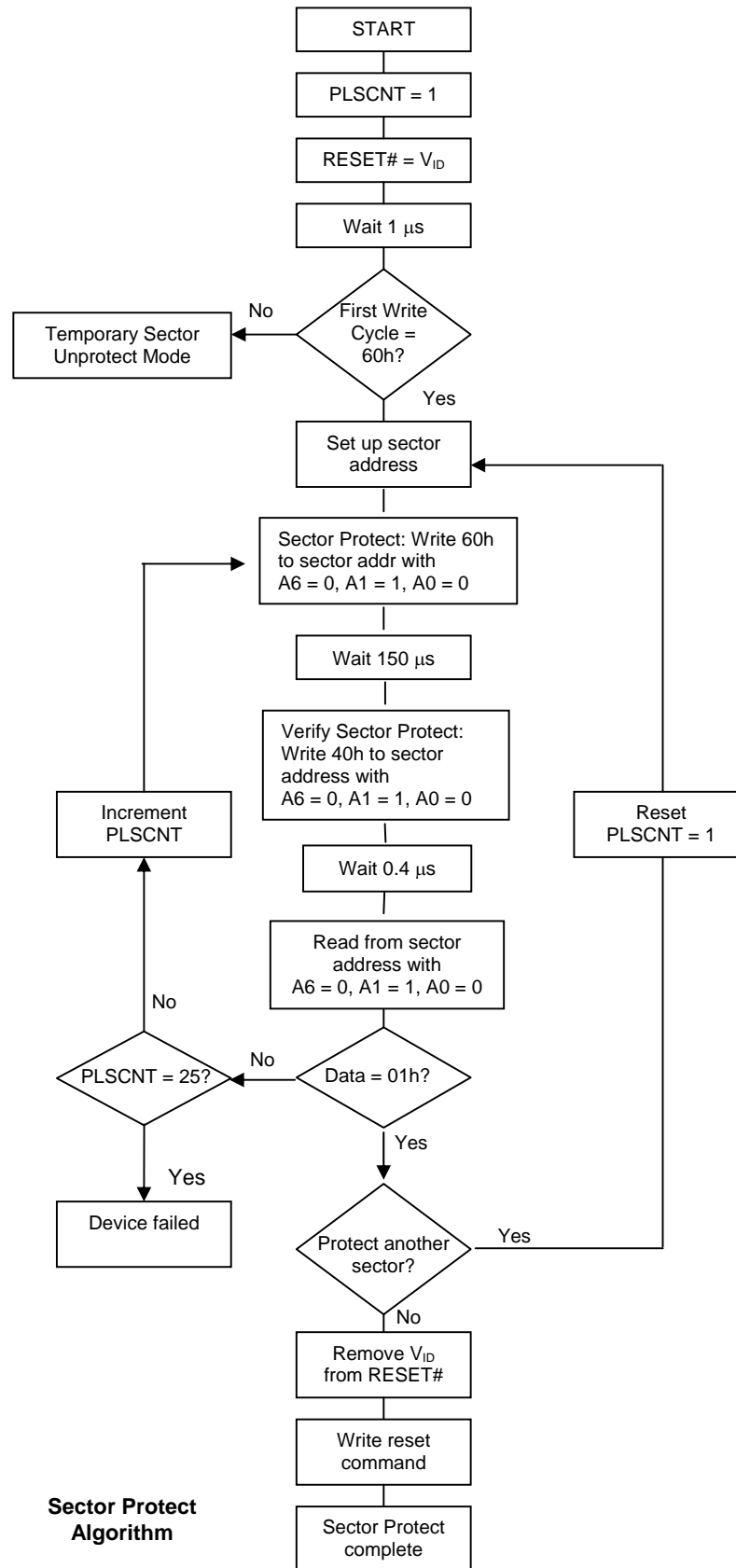
Chip Erase

Sector Erase


Flowchart 5. DATA# Polling Algorithm

Notes:

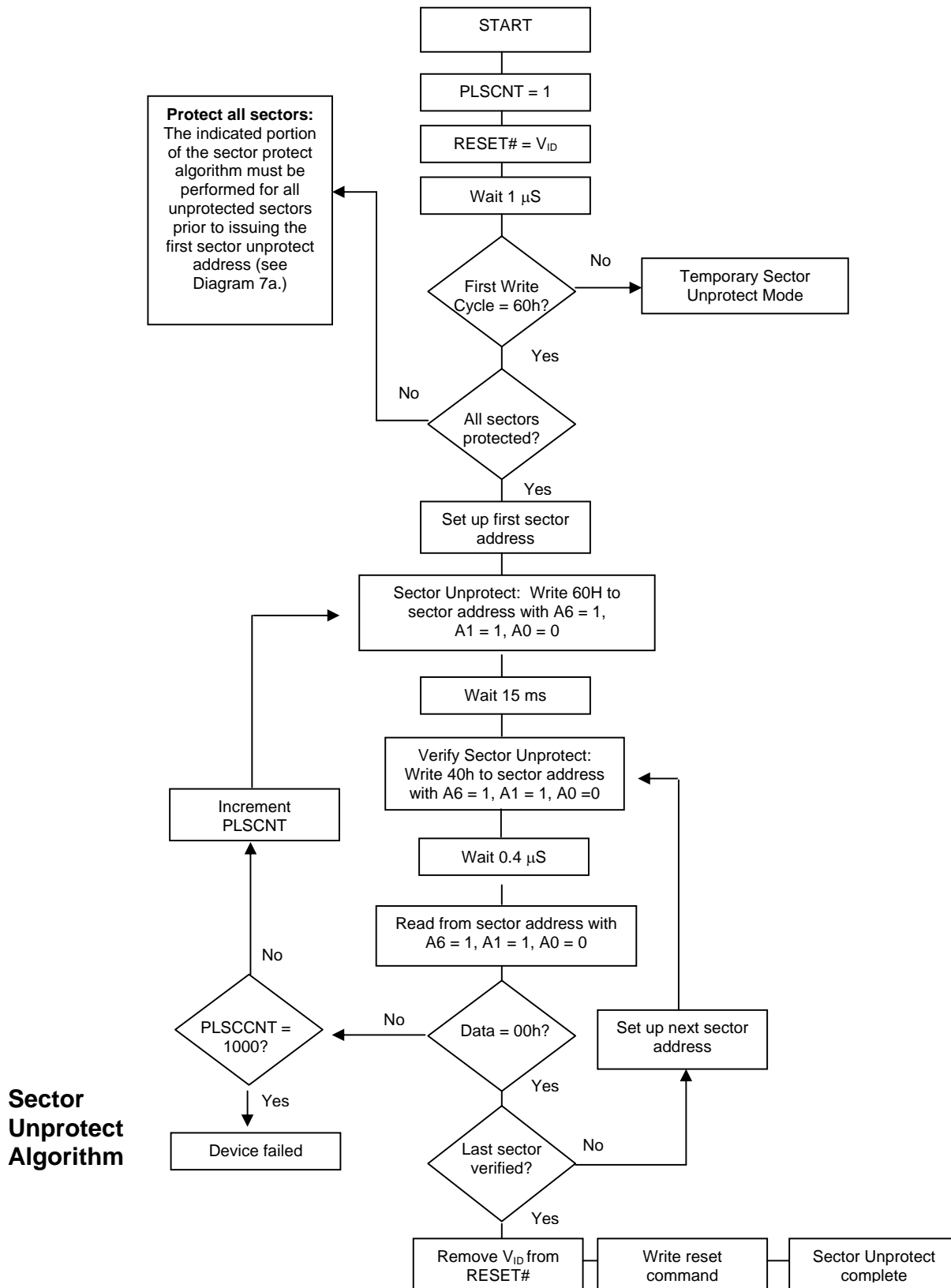
(1) This second read is necessary in case the first read was done at the exact instant when the status data was in transition.

Flowchart 6. Toggle Bit Algorithm

Notes:

(2) This second set of reads is necessary in case the first set of reads was done at the exact instant when the status data was in transition.

Flowchart 7a. In-System Sector Protect Flowchart


Flowchart 7b. In-System Sector Unprotect Flowchart

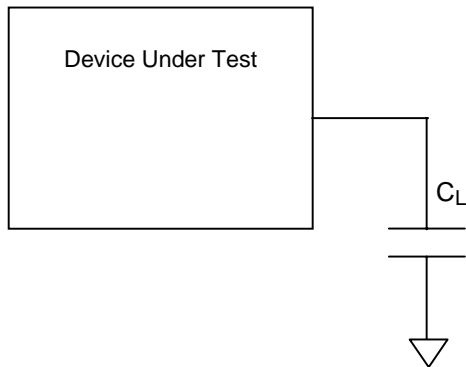


**Table 7. DC Characteristics** $(T_a = 0^\circ\text{C to } 70^\circ\text{C or } -40^\circ\text{C to } 85^\circ\text{C}; V_{CC} = 2.7\text{-}3.6\text{V})$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$			± 1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$			± 1	μA
I_{CC1}	Supply Current (read) CMOS Byte	$CE\# = V_{IL}; OE\# = V_{IH};$ $f = 5\text{MHz}$		6	12	mA
	(read) CMOS Word			7	12	mA
I_{CC2}	Supply Current (Standby - CMOS)	$CE\# = \text{BYTE}\# =$ $RESET\# = V_{CC} \pm 0.3\text{V}$ (Note 1)		1	5.0	μA
I_{CC3}	Supply Current (Program or Erase)	Byte program, Sector or Chip Erase in progress		15	30	mA
I_{CC4}	Automatic Sleep Mode	$V_{IH} = V_{CC} \pm 0.3\text{V}$ $V_{IL} = V_{SS} \pm 0.3\text{V}$		1	5.0	μA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		$0.7 \times$ V_{CC}		$V_{CC} \pm$ 0.3	V
V_{OL}	Output Low Voltage	$I_{OL} = 4.0\text{ mA}$			0.45	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = -100\ \mu\text{A},$	$V_{CC} -$ 0.4V			V
V_{ID}	A9 Voltage (Electronic Signature)		10.5		11.5	V
I_{ID}	A9 Current (Electronic Signature)	$A9 = V_{ID}$			100	μA
V_{LKO}	Supply voltage (Erase and Program lock-out)		2.3		2.5	V

Notes

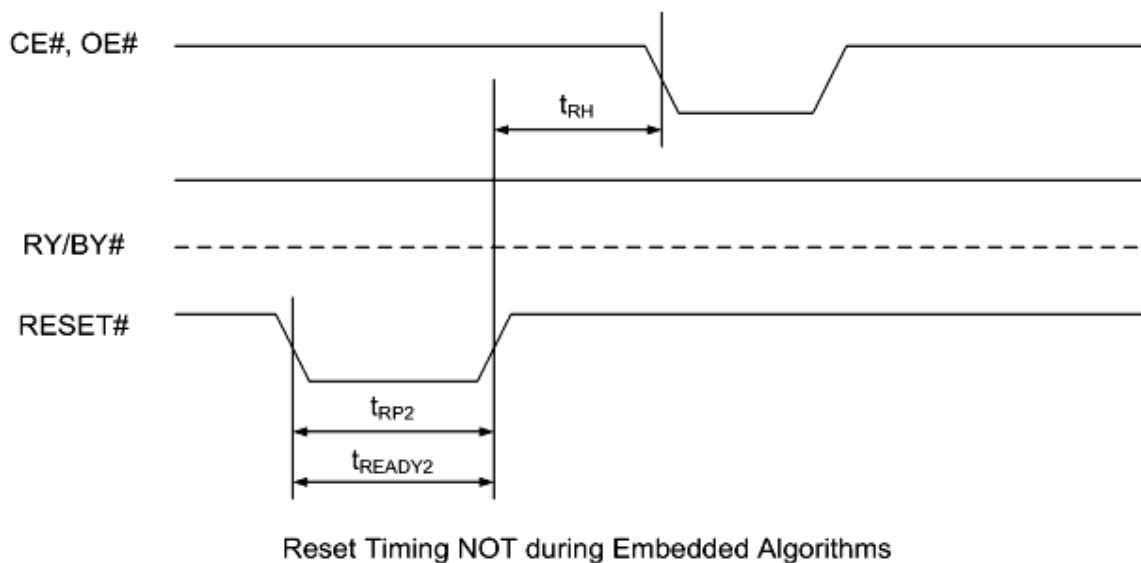
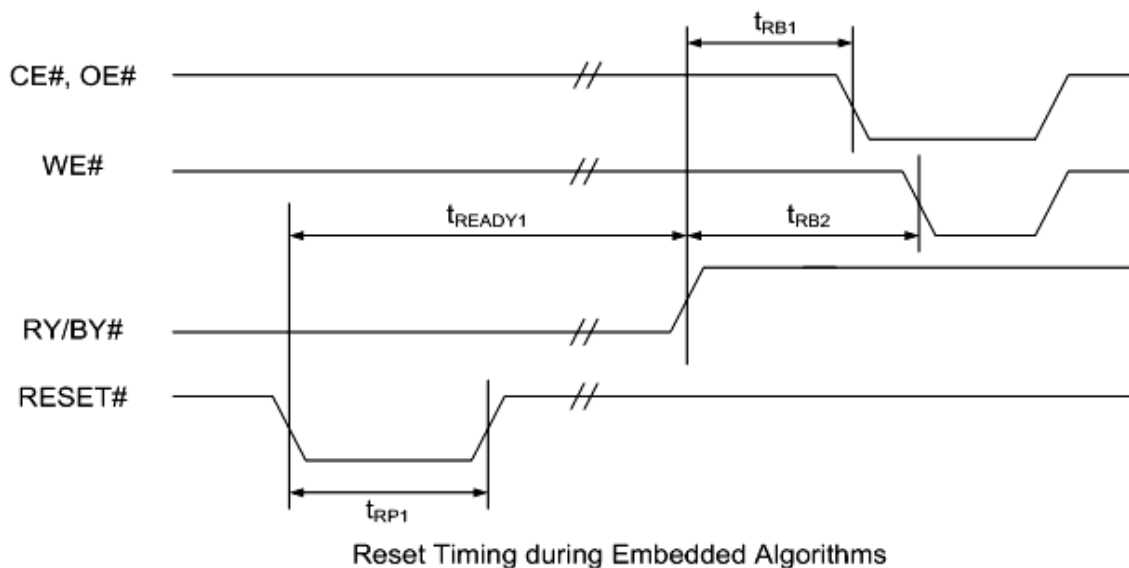
1. BYTE# pin can also be $\text{GND} \pm 0.3\text{V}$. BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.

Test Conditions

Test Specifications

Test Conditions	-45R	-55R	-70	Unit
Output Load Capacitance, C_L	30	30	30	pF
Input Rise and Fall times	5	5	5	ns
Input Pulse Levels	0.0-3.0	0.0-3.0	0.0-3.0	V
Input timing measurement reference levels	1.5	1.5	1.5	V
Output timing measurement reference levels	1.5	1.5	1.5	V

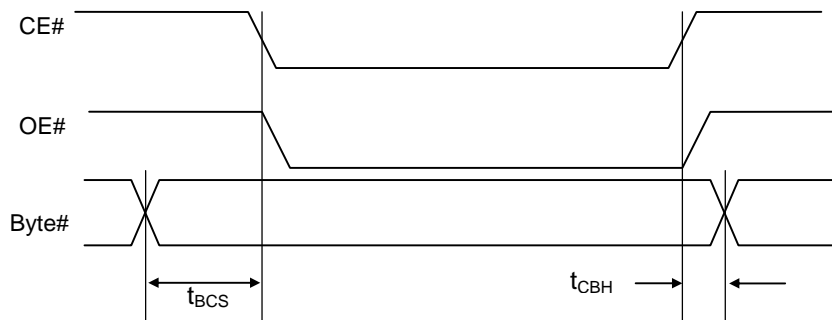
AC CHARACTERISTICS
Hardware Reset (Reset#)

Parameter Std	Description	Test Setup	Speed			Unit
			-45R	-55R	-70	
t_{RP1}	RESET# Pulse Width (During Embedded Algorithms)	Min	10			us
t_{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	Min	500			ns
t_{RH}	Reset# High Time Before Read	Min	50			ns
t_{RB1}	RY/BY# Recovery Time (to CE#, OE# go low)	Min	0			ns
t_{RB2}	RY/BY# Recovery Time (to WE# go low)	Min	50			ns
t_{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	Max	20			us
t_{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	Max	500			ns

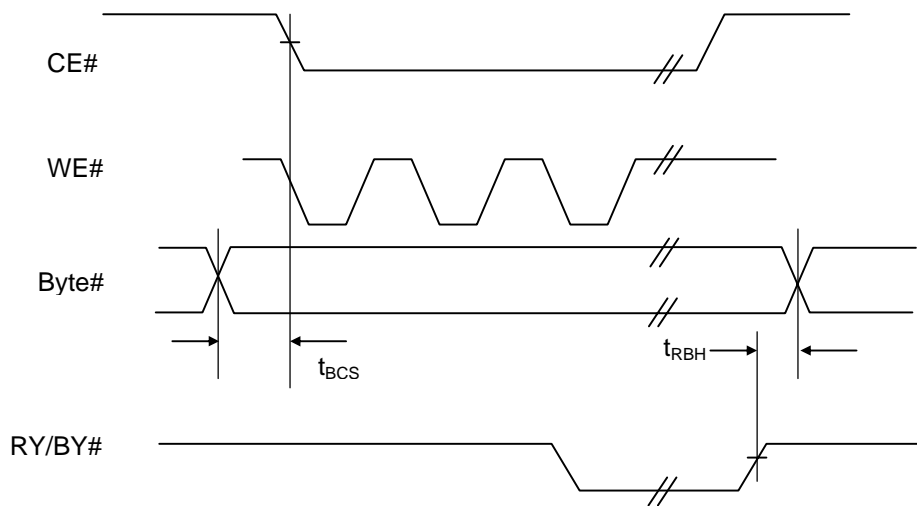
Figure 1. AC Waveforms for RESET#
Reset# Timings


AC CHARACTERISTICS
Word / Byte Configuration (Byte#)

Std Parameter	Description		Speed			Unit
			-45R	-55R	-70	
t_{BCS}	Byte# to CE# switching setup time	Min	0	0	0	ns
t_{CBH}	CE# to Byte# switching hold time	Min	0	0	0	ns
t_{RBH}	RY/BY# to Byte# switching hold time	Min	0	0	0	ns

Figure 2. AC Waveforms for BYTE#


Byte# timings for Read Operations



Byte #timings for Write Operations

Note: Switching BYTE# pin not allowed during embedded operations

Table 8. AC CHARACTERISTICS
Read-only Operations Characteristics

Parameter Symbols		Description	Test Setup		Speed Options			Unit
JEDEC	Standard				-45R	-55R	-70	
t_{AVAV}	t_{RC}	Read Cycle Time		Min	45	55	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	Max	45	55	70	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay	OE# = V_{IL}	Max	45	55	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	30	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z		Max	10	15	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z		Max	10	15	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, whichever occurs first		Min	0	0	0	ns
	t_{OEh}	Output Enable Hold Time	Read	Min	0	0	0	ns
			Toggle and Data# Polling	Min	10	10	10	ns

Notes:

- High Z is Not 100% tested.
- For -45R,-55R,70 $V_{CC} = 3.0V \pm 5\%$ Output Load : 30pF
 Input Rise and Fall Times: 5ns Input Rise Levels: 0.0 V to V_{CC}
 Timing Measurement Reference Level, Input and Output: 1.5 V

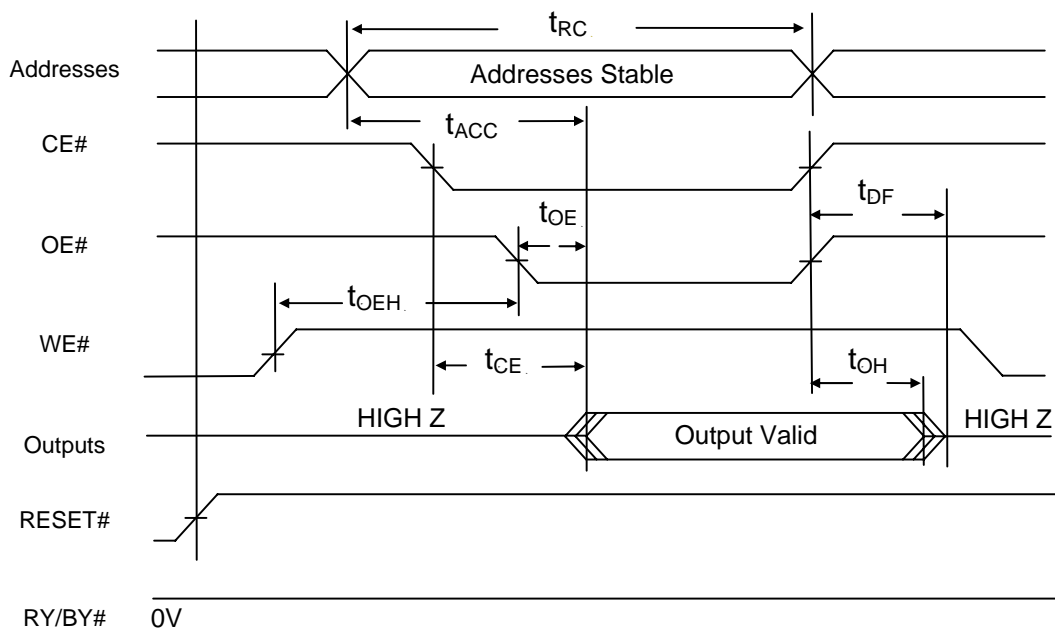
Figure 3. AC Waveforms for READ Operations




Table 9. AC CHARACTERISTICS

Write (Erase/Program) Operations

Parameter Symbols		Description		Speed Options			Unit	
JEDEC	Standard			-45R	-55R	-70		
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	55	70	ns	
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	ns	
t_{WLAX}	t_{AH}	Address Hold Time	Min	35	45	45	ns	
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	25	30	ns	
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	ns	
	t_{OES}	Output Enable Setup Time	Min	0	0	0	ns	
	t_{OEHL}	Output Enable Hold Time	Read	Min	0	0	0	ns
			Toggle and Data# Polling	Min	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write (OE# High to WE# Low)	Min	0	0	0	ns	
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	0	0	ns	
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	0	0	ns	
t_{WLWH}	t_{WP}	Write Pulse Width	Min	25	30	35	ns	
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	20	20	20	ns	
t_{WHWH1}	t_{WHWH1}	Programming Operation (Word AND Byte Mode) (Note 2)	Typ	8	8	8	μ s	
			Max	300	300	300	μ s	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	0.5	0.5	s	
	t_{VCS}	Vcc Setup Time	Min	50	50	50	μ s	
	t_{VIDR}	Rise Time to VID	Min	500	500	500	ns	
	t_{RB}	Recovery Time from RY/BY#	Min	0	0	0	ns	
	t_{BUSY}	WE# High to RY/BY# Low	Max	45	55	70	ns	

Notes:

1. Not 100% tested.
2. See Erase and Programming Performance for more information.



Table 10. AC CHARACTERISTICS
Write (Erase/Program) Operations
 Alternate CE# Controlled Writes

Parameter Symbols				Speed Options			
JEDEC	Standard	Description		-45R	-55R	-70	Unit
t _{AVAV}	t _{WC}	Write Cycle Time (Note 1)	Min	45	55	70	ns
t _{AVEL}	t _{AS}	Address Setup Time	Min	0	0	0	ns
t _{ELAX}	t _{AH}	Address Hold Time	Min	35	45	45	ns
t _{DVEH}	t _{DS}	Data Setup Time	Min	20	25	30	ns
t _{EHDX}	t _{DH}	Data Hold Time	Min	0	0	0	ns
	t _{OES}	Output Enable Setup Time	Min	0	0	0	ns
	t _{OEHL}	Output Enable Hold Time	Read	Min	0	0	ns
			Toggle and Data# Polling	Min	10	10	10
t _{GHEL}	t _{GHEL}	Read Recovery Time before Write (OE High to CE Low)	Min	0	0	0	ns
t _{WLEL}	t _{WS}	WE# SetupTime	Min	0	0	0	ns
t _{EHWH}	t _{WH}	WE# Hold Time	Min	0	0	0	ns
t _{ELEH}	t _{CP}	Write Pulse Width	Min	25	30	35	ns
t _{EHEL}	t _{CPH}	Write Pulse Width High	Min	20	20	20	ns
t _{WHWH1}	t _{WHWH1}	Programming Operation (byte AND word mode) (Note 2)	Typ	8	8	8	μs
			Max	300	300	300	μs
t _{WHWH2}	t _{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	0.5	0.5	s
	t _{VCS}	Vcc Setup Time	Min	50	50	50	μs
	t _{VIDR}	Rise Time to V _{ID}	Min	500	500	500	ns
	t _{RB}	Recovery Time from RY/BY#	Min	0	0	0	ns

Notes:

1. Not 100% tested.
2. See Erase and Programming Performance for more information.

**Table 11. ERASE AND PROGRAMMING PERFORMANCE**

Parameter	Limits			Comments
	Typ	Max	Unit	
Sector Erase Time	0.5	10	sec	Excludes 00H programming prior to erasure
Chip Erase Time	5	100	sec	
Byte Programming Time	8	300	μs	Excludes system level overhead
Word Programming Time	8	300	μs	
Chip Programming Time	Byte	4.2	12.6	
	Word	2.1	6.3	
Erase/Program Endurance	100K		cycles	Minimum 100K cycles

Table 12. TSOP PIN CAPACITANCE @ 25°C, 1.0MHz

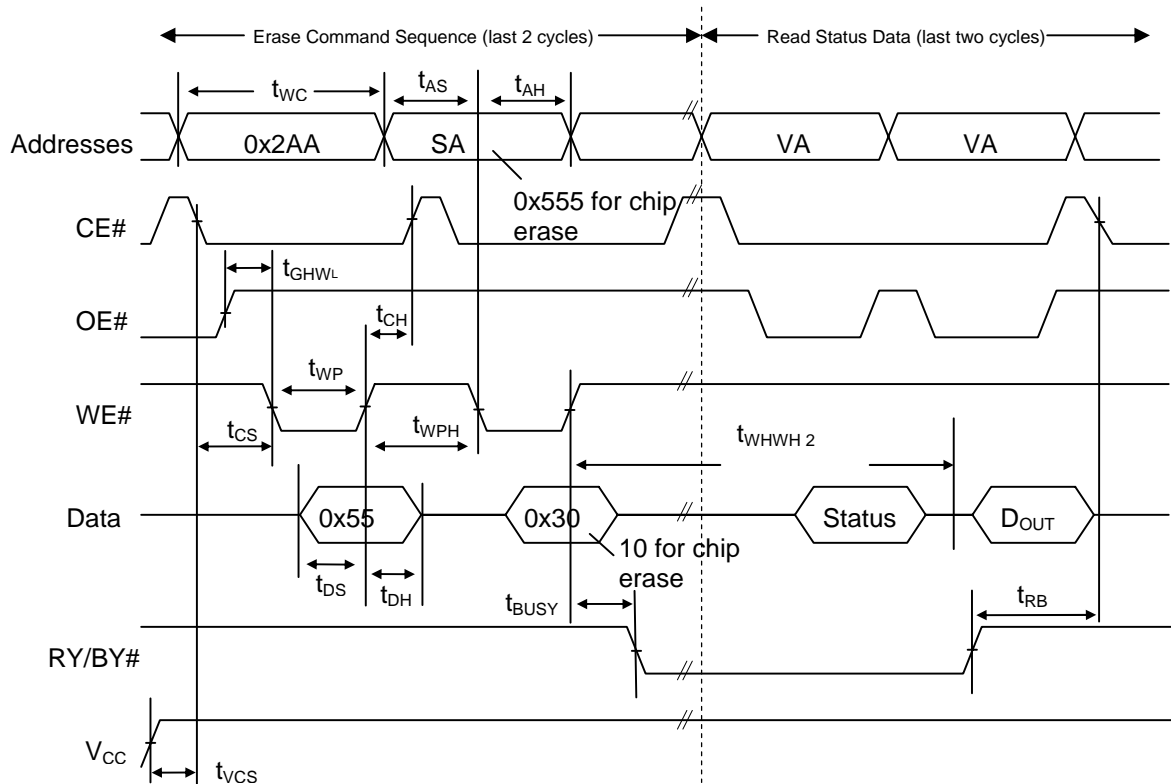
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	7.5	9	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8	10	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	9.5	12.5	pF

Table 13. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years

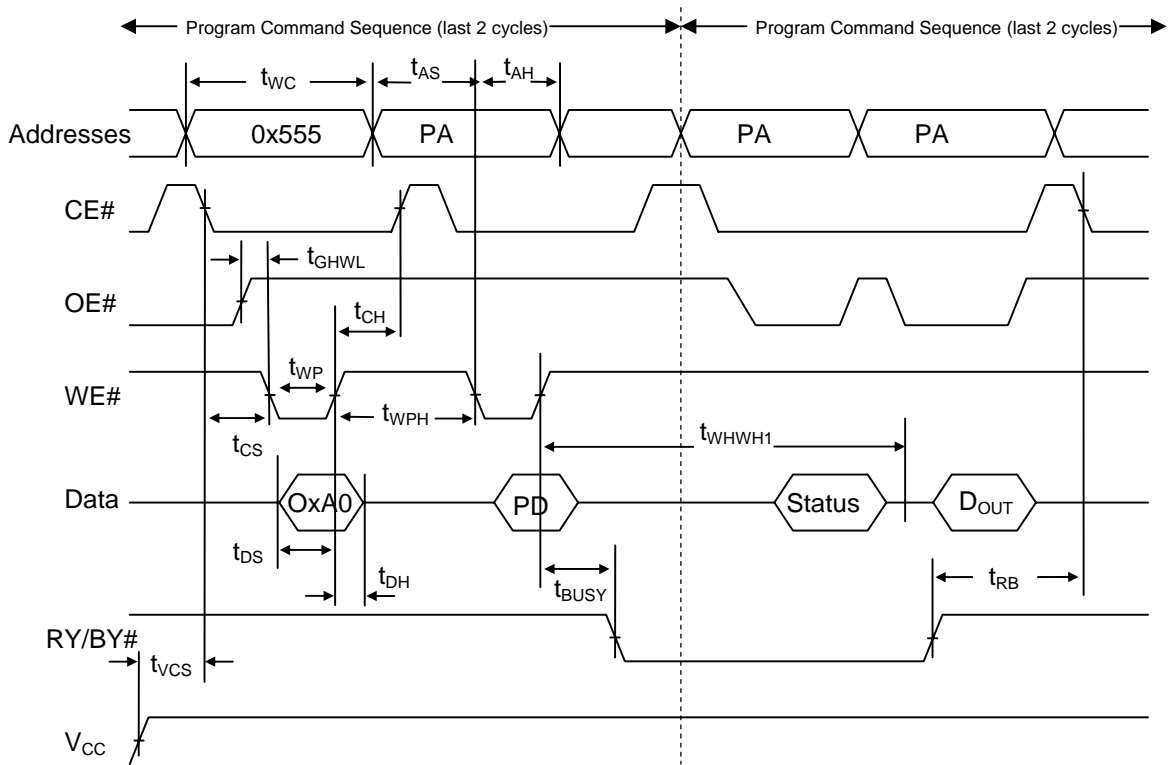
AC CHARACTERISTICS

Figure 4. AC Waveforms for Chip/Sector Erase Operations Timings

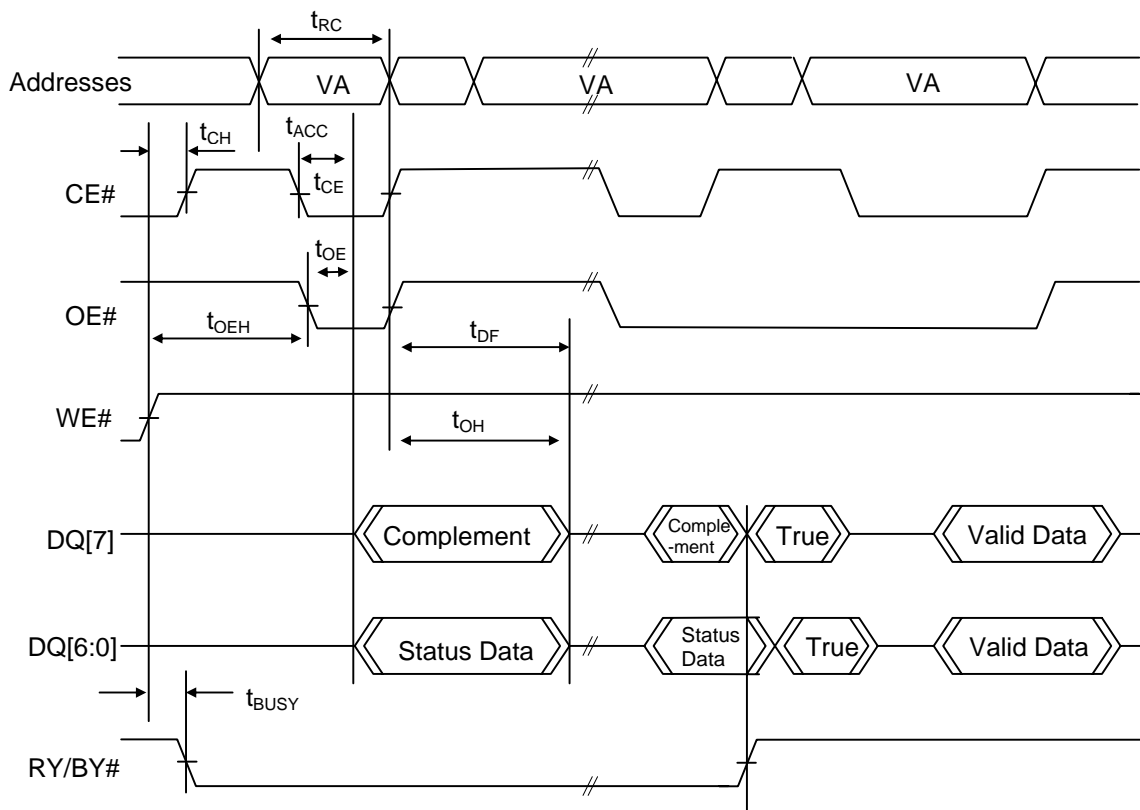


Notes:

1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 5. Program Operation Timings

Notes:

1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 6. AC Waveforms for DATA# Polling During Embedded Algorithm Operations

Notes:

1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

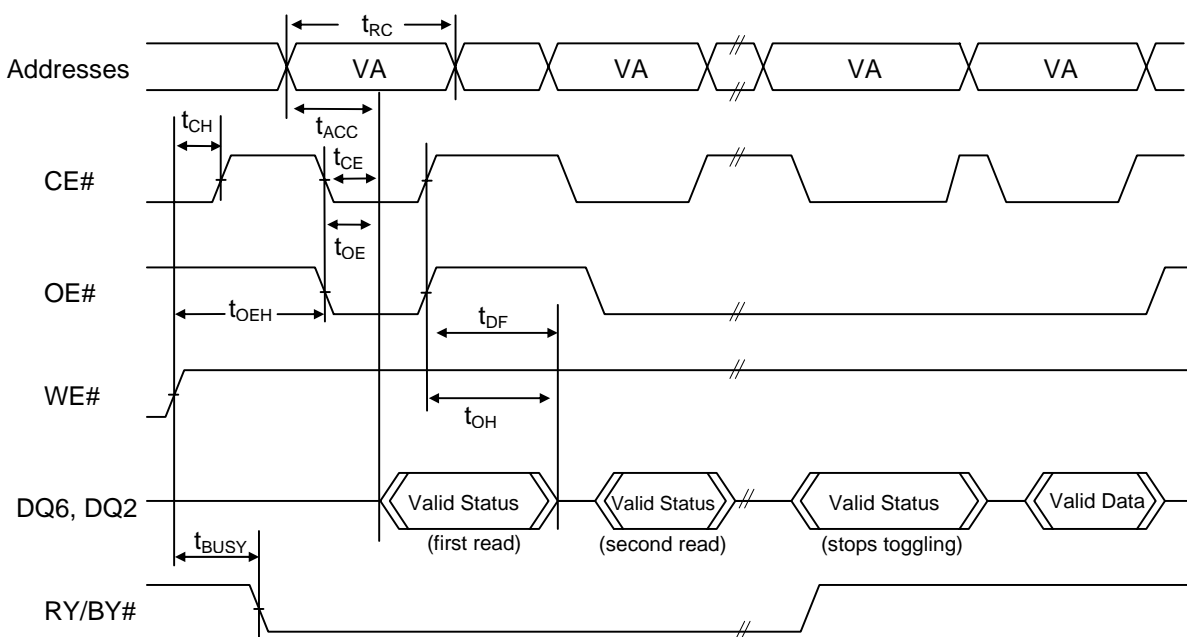
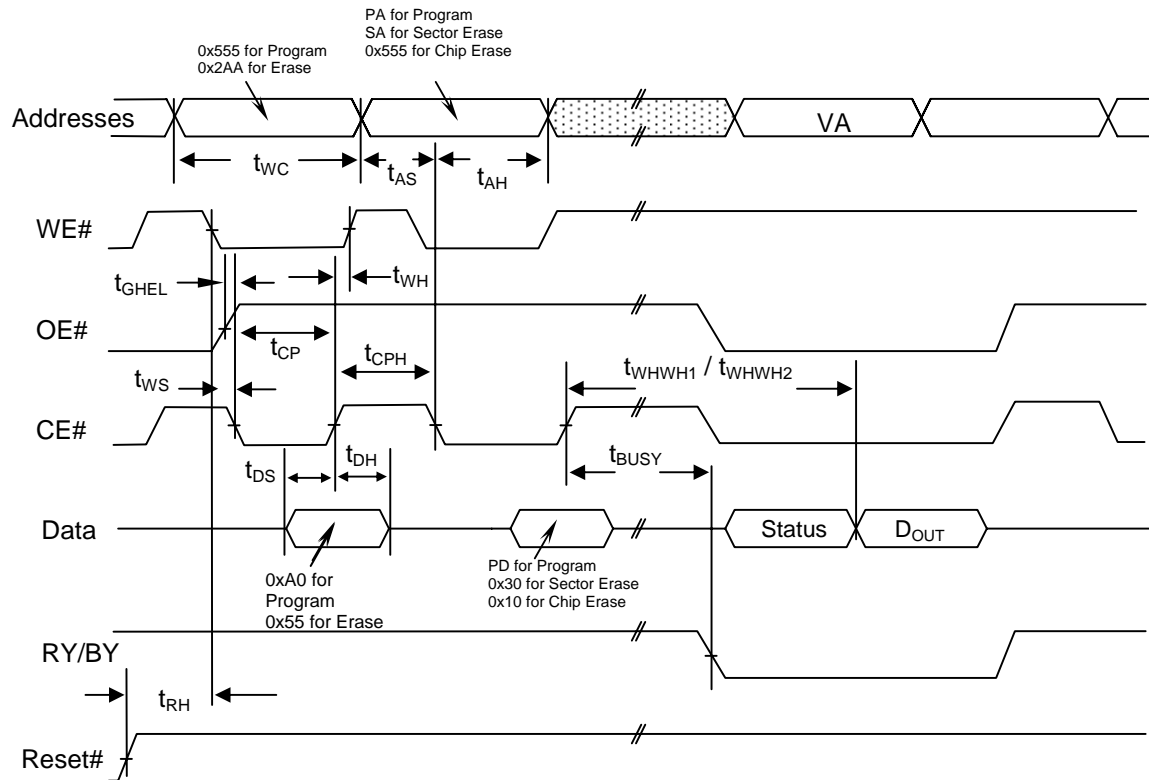
Figure 7. AC Waveforms for Toggle Bit During Embedded Algorithm Operations


Figure 8. Alternate CE# Controlled Write Operation Timings

Notes:

PA = address of the memory location to be programmed.
 PD = data to be programmed at byte address.
 VA = Valid Address for reading program or erase status
 D_{out} = array data read at VA
 Shown above are the last two cycles of the program or erase command sequence and the last status read cycle
 Reset# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

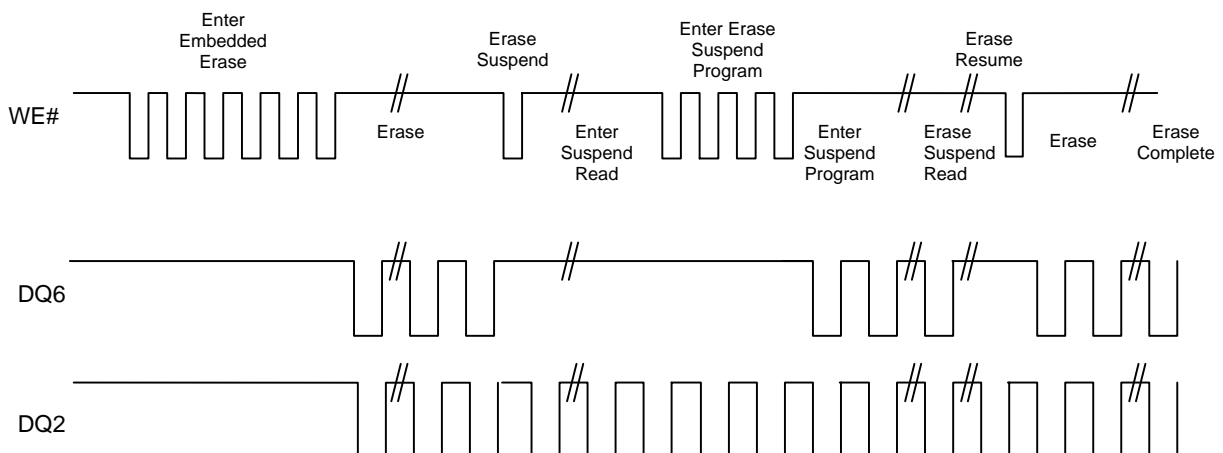
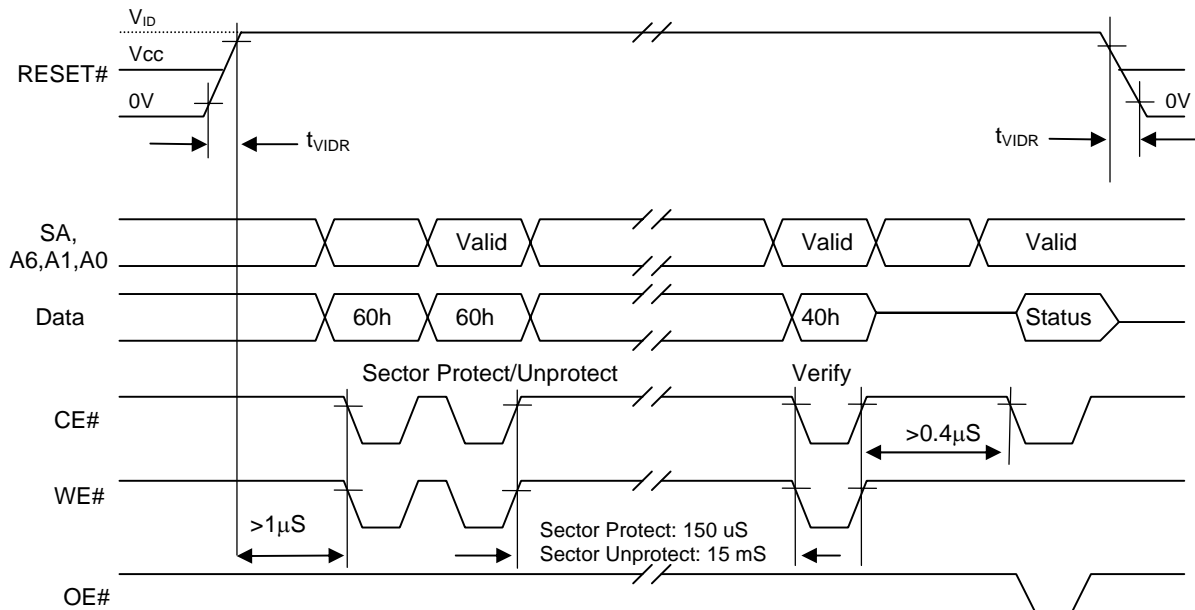
Figure 9. DQ2 vs. DQ6


Figure 10. Sector Protect/Unprotect Timing Diagram

Notes:

Use standard microprocessor timings for this device for read and write cycles.
 For Sector Protect, use A6=0, A1=1, A0=0. For Sector Unprotect, use A6=1, A1=1, A0=0.

Temporary Sector Unprotect

Parameter Std	Description		Speed Option			Unit
			-45R	-55R	-70	
t_{VIDR}	V_{ID} Rise and Fall Time	Min	500			ns
t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4			μ s

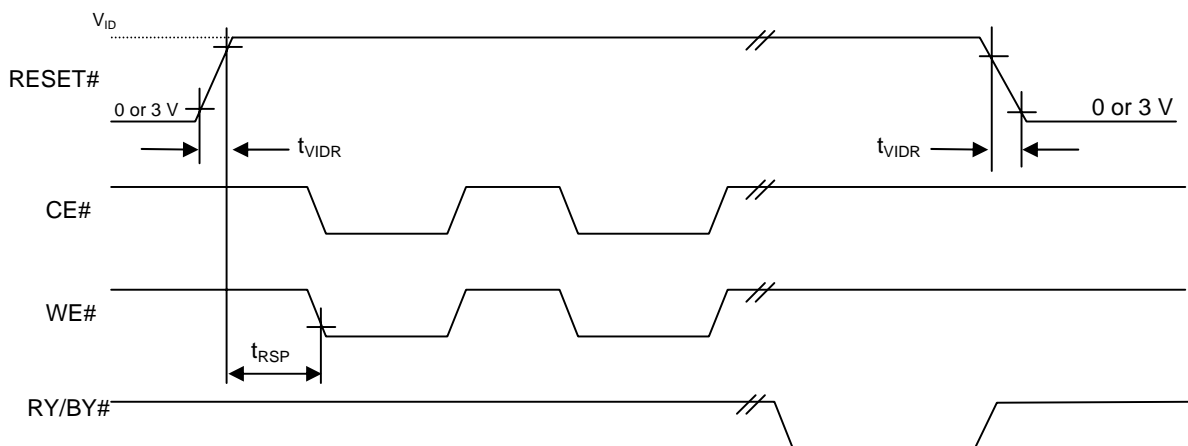
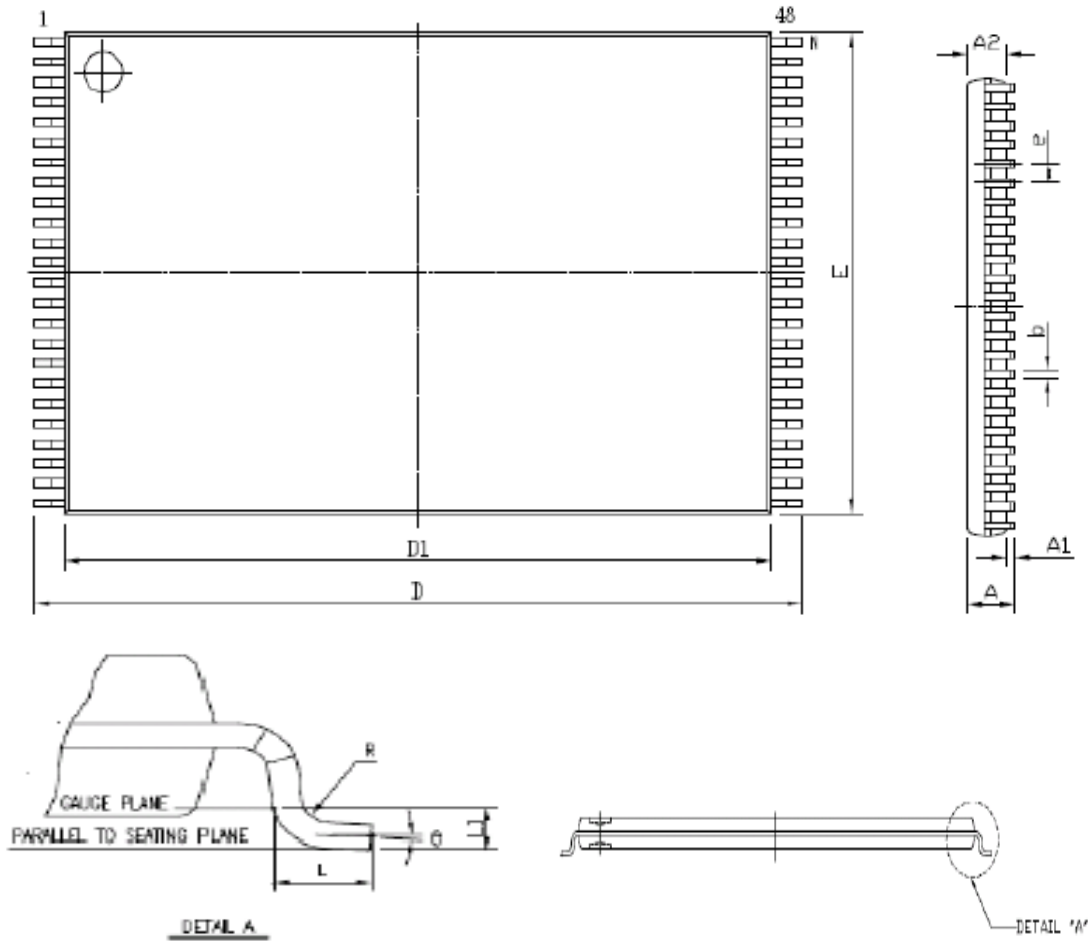
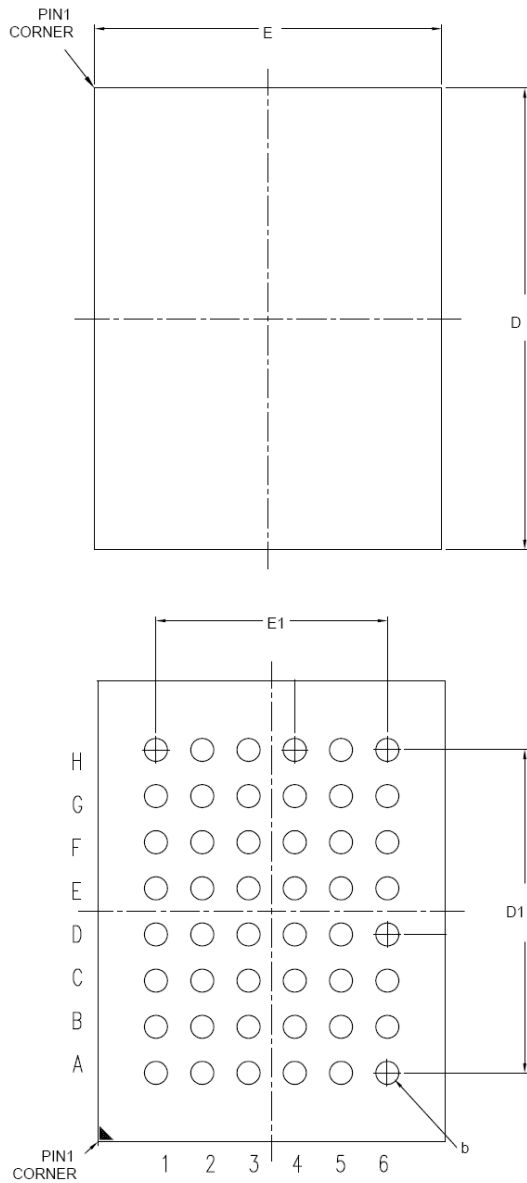
Figure 11. Temporary Sector Unprotect Timing Diagram


FIGURE 12. 48L TSOP 12mm x 20mm package outline


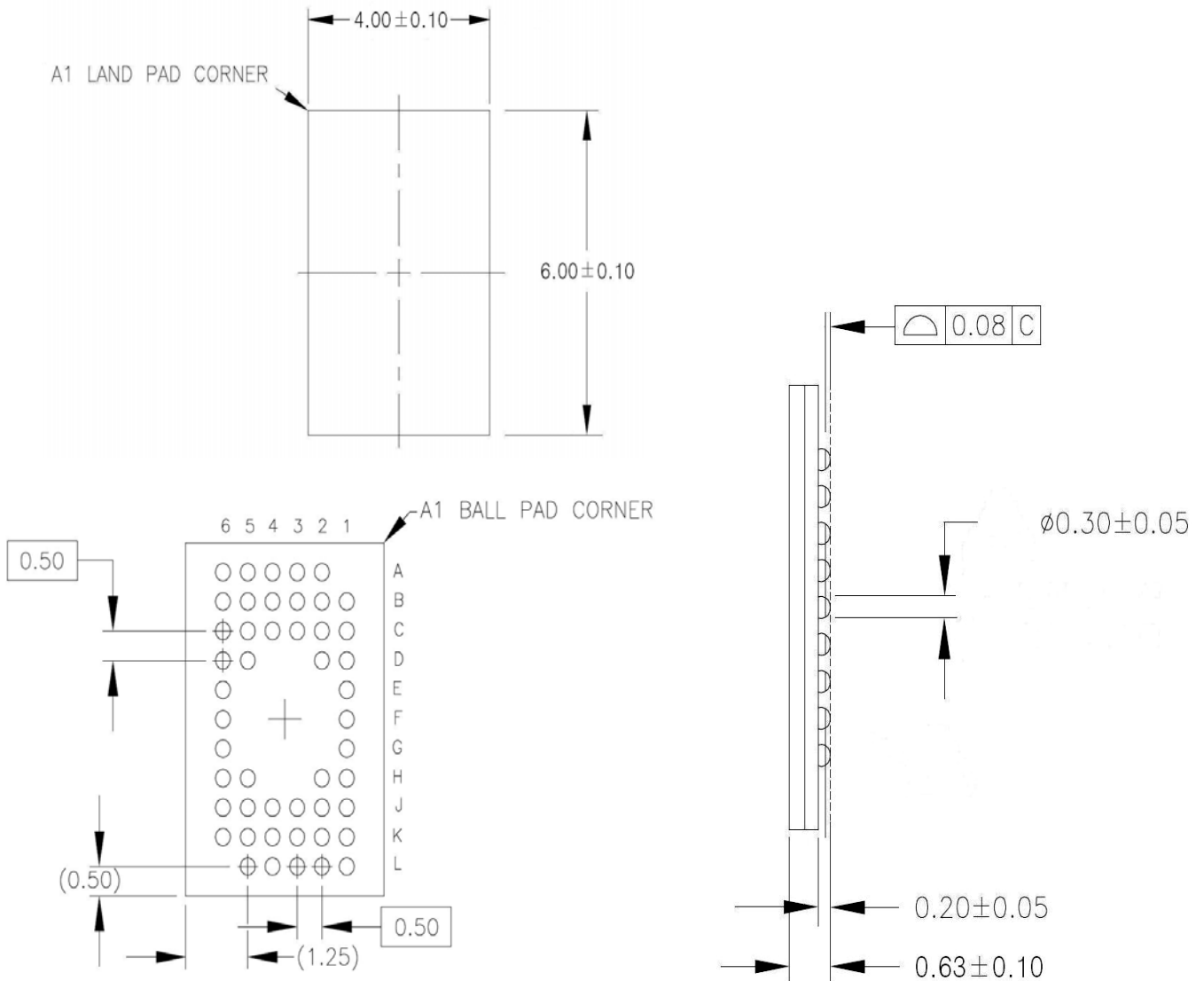
SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.9	12.00	12.10
e	---	0.50	---
b	0.17	0.22	0.27
L	0.5	0.60	0.70
L1	---	0.25	---
R	0.08	---	0.20
θ	0°	3°	5°

Note : 1. Coplanarity: 0.1 mm
 2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

FIGURE 13. 48L TFBGA 6mm x 8mm package outline


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	---	---	1.30
A1	0.23	0.29	---
A2	0.84	0.91	---
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	---	5.60	---
E1	---	4.00	---
e	---	0.80	---
b	0.35	0.40	0.45

Note : 1. Coplanarity: 0.1 mm

Figure 14. 48L WFBGA 4mm x 6mm package outline


Note : Controlling dimensions are in millimeters (mm).

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit	
Storage Temperature	-65 to +150	°C	
Plastic Packages	-65 to +125	°C	
Ambient Temperature With Power Applied	-55 to +125	°C	
Output Short Circuit Current ¹	200	mA	
Voltage with Respect to Ground	A9, OE#, Reset# ²	-0.5 to +11.5	V
	All other pins ³	-0.5 to V _{cc} +0.5	V
	V _{cc}	-0.5 to +4.0	V

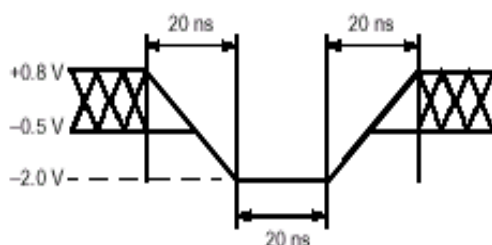
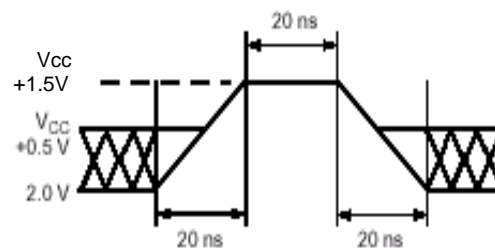
Notes:

- No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
- Minimum DC input voltage on A9, OE#, RESET# pins is -0.5V. During voltage transitions, A9, OE#, RESET# pins may undershoot V_{ss} to -1.0V for periods of up to 50ns and to -2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 10.5V which may overshoot to 11.5V for periods up to 20ns.
- Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, inputs may undershoot V_{ss} to -1.0V for periods of up to 50ns and to -2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.
- Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

RECOMMENDED OPERATING RANGES¹

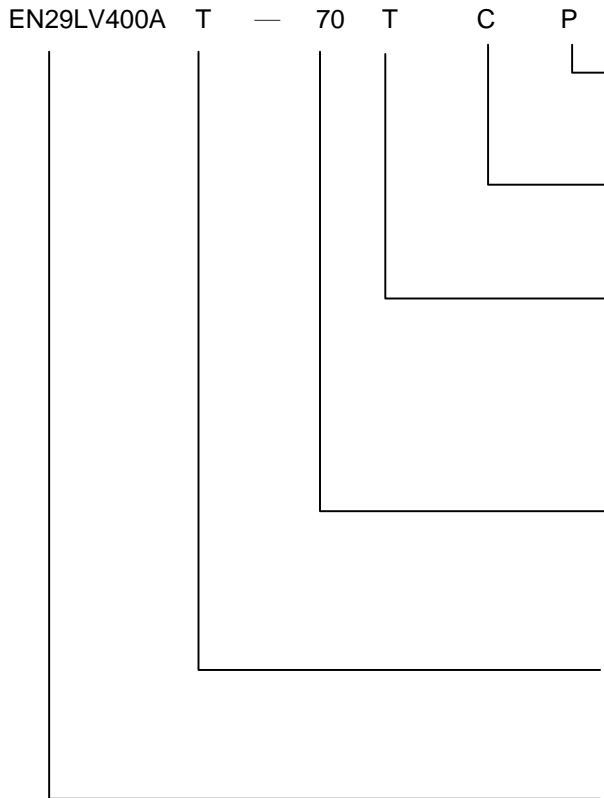
Parameter	Value	Unit
Ambient Operating Temperature Commercial Devices Industrial Devices	0 to 70 -40 to 85	°C
Operating Supply Voltage V _{cc}	Regulated Voltage Range: 3.0-3.6	V
	Standard Voltage Range: 2.7 to 3.6	

- Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.


 Maximum Negative Overshoot
Waveform

 Maximum Positive Overshoot
Waveform



ORDERING INFORMATION



PACKAGING CONTENT

P = RoHS compliant

TEMPERATURE RANGE

C = Commercial (0°C to +70°C)

I = Industrial (-40°C to +85°C)

PACKAGE

T = 48-pin TSOP

B = 48-ball Thin Fine Pitch Ball Grid Array (TFBGA)
0.80mm pitch, 6mm x 8mm package

N = 48-Ball Very-Very-Thin-Profile Fine Pitch
Ball Grid Array (WFBGA)
0.5mm pitch, 4mm x 6mm package

SPEED

45R = 45ns Regulated range 3.0V~3.6V

55R = 55ns Regulated range 3.0V~3.6V

70 = 70ns

BOOT CODE SECTOR ARCHITECTURE

T = Top Sector

B = Bottom Sector

BASE PART NUMBER

EN = Eon Silicon Solution Inc.

29LV = FLASH, 3V Read Program Erase

400 = 4 Megabit (512K x 8 / 256K x 16)

A = Version Identifier



Revisions List

Revision No	Description	Date
A	Initial Release	2004/01/07
B	<ol style="list-style-type: none">1. Correct the typo of program/erase Endurance cycle to 100K at FEATURES page 12. Change the FBGA package dimension to enhance the BGA substrate and ball strength, the difference is Package Thickness A : 1.10 mm to 1.31 mm Ball size b : 0.3 mm to 0.4 mm	2005/11/8
C	<ol style="list-style-type: none">1. Remove ,Unlock Bypass, Unlock Bypass Program, and Unlock Bypass Reset, commands from Table 9.2. Remove description of Unlock Bypass	2006/02/21
D	<ol style="list-style-type: none">1. Add the t_{BUSY} description in Table 9. Write (Erase/Program) Operations in page 282. Correct the Figure 7. Program Operation Timings in page 323. Update 48 pin TSOP-I package outline in page 364. Change the FBGA 48 Ball package thickness from 1.31mm to 1.30mm in page 37	2008/04/25
E	Add Eon products' New top marking "cFeon" information in page 1.	2009/01/09
F	<ol style="list-style-type: none">1. Add 48-ball 4mm x 6mm WFBGA package option.2. Modify Table 6 Status Register Bits DQ5 from ERROE BIT to TIME OUT BIT on page 19.3. Modify Test Conditions illustration on page 26.4. Update Hardware Reset (RESET#) table and Figure 1. AC Waveforms for RESET# on page 27.5. Modify Storage Temperature from "-65 to + 125" to "-65 to +150" on page 41.6. Modify P = Pb free to P = RoHS compliant on page 42.7. Remove the Latch up Characteristics Table.	2009/09/24
G	<ol style="list-style-type: none">1. Add the chip will output a configuration code 7Fh,if a manufacturing ID is read with A8=L (000h).2. Remove the speed option of 90ns.	2011/01/04